



# UHiFET – A New High-Frequency High-Voltage Device

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# Outline

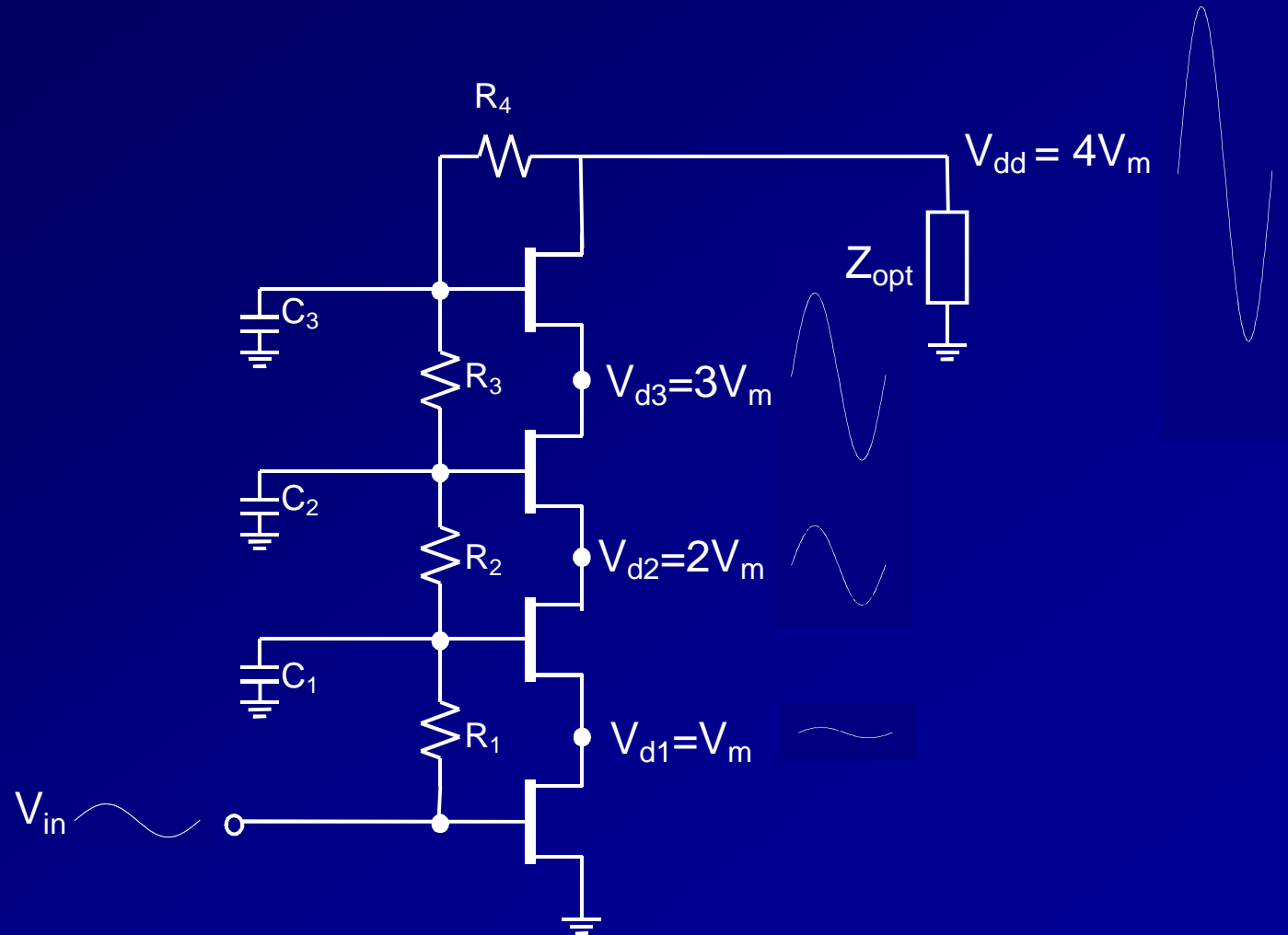
- Introduction
- Universal High-Voltage FET (UHiFET)
- Theoretical Considerations
- UHiFET Experimental Verification
- Conclusion

# Introduction

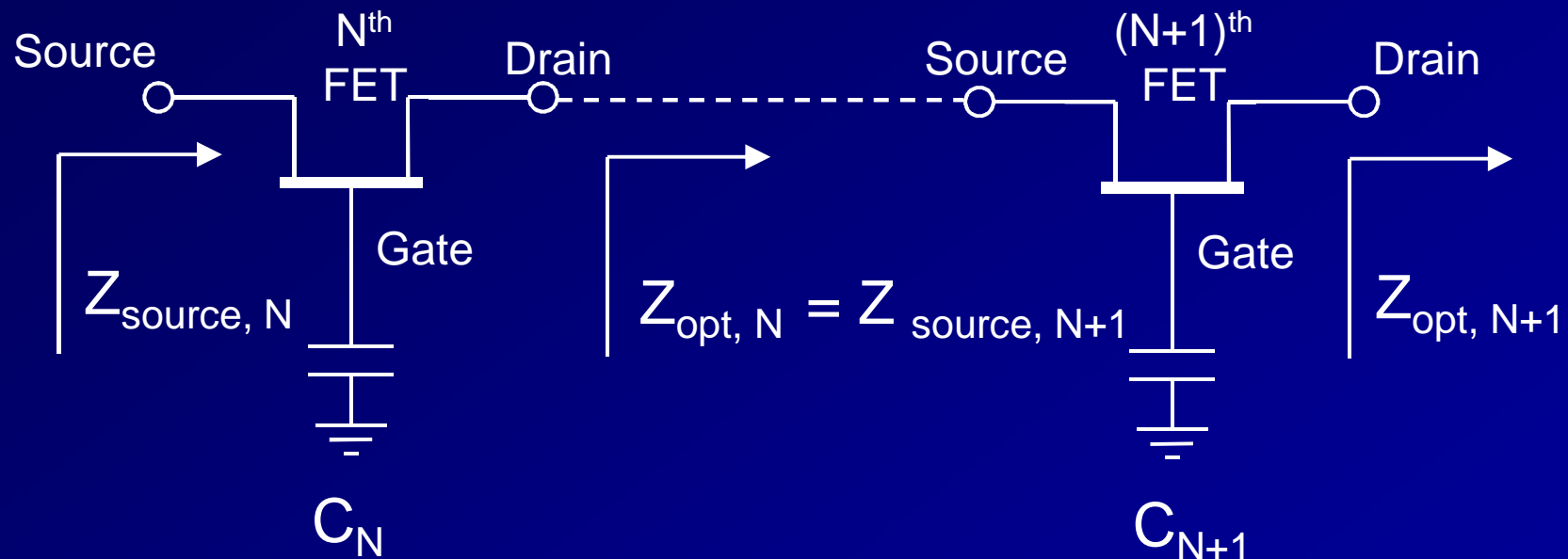
# Background

- The High-Voltage/Power Device (HiVP) is a technique used for combining several FETs DC and RF in series
- HiVP is useful for applications requiring high voltage and high power particularly at frequencies below 3GHz using semiconductors devices with low breakdown voltage such as: CMOS & GaAs
- HiVP concept was verified to build broadband high power GaAs MMICs up to C-Band as well as Si MMICs
- HiVP concept suffers from power and efficiency degradation at high frequencies (i.e.  $> 3\text{GHz}$ ) because the FETs in series get into different phases and their powers do not add efficiently

# 4-Cell High Voltage/ High Power (HiVP)



# Impedance Optimization of HiVP



$$Z_{\text{source}, N} = 1 / (g_m + j \omega C_{gs}) (C_{gs} + C_N) / C_N$$

$$Z_{\text{source}, N} \cong 1 / g_m (C_{gs} + C_N) / C_N \text{ (at low frequencies)}$$

$g_m$  is FET trans-conductance

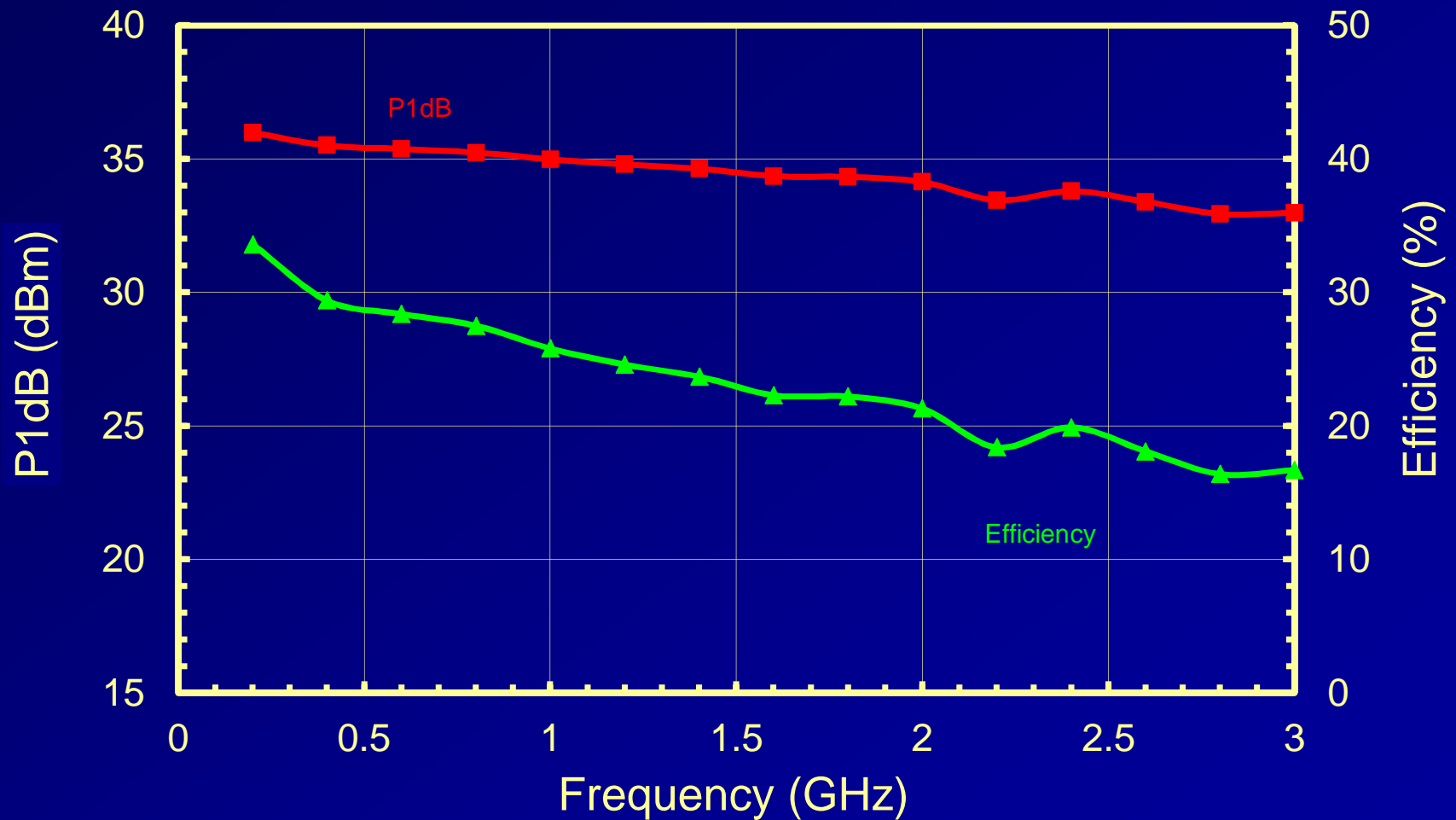
$C_{gs}$  is FET gate-to-source capacitance

# Merits and Restrictions of HiVP

- Equivalent performance to a single large device:
  - Efficiency
  - Power
- High voltage bias:  $V_{dd} = V_{ds} \times N$
- Lower Current by  $1/N$  factor compared to regular FET with equivalent periphery
- Higher optimum output impedance by  $N^2$  factor
- Higher input impedance by a factor of  $N$
- Higher gain by factor of  $N$
- However due to gate current leakage the HiFET output power degrades at higher frequencies

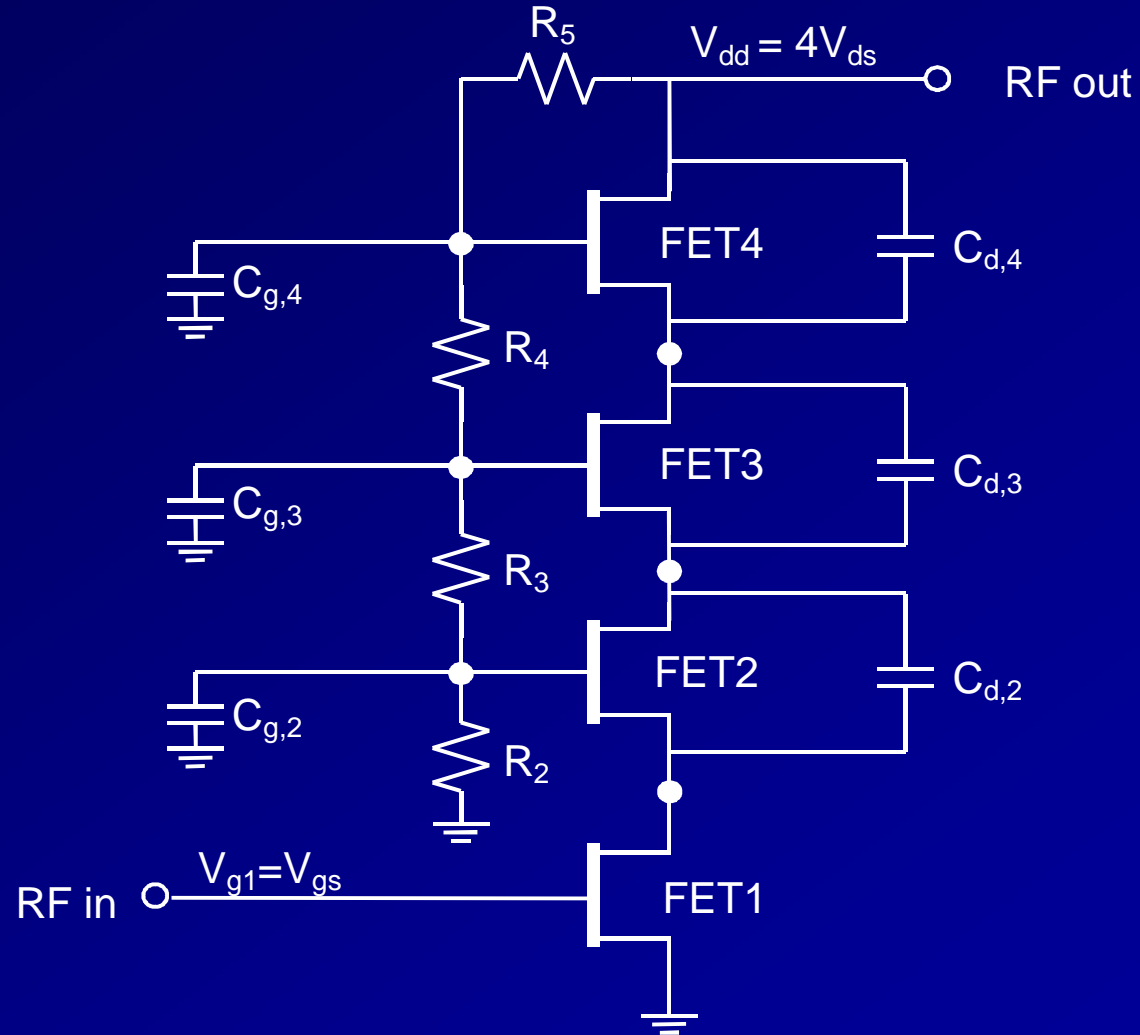
# Typical Power of a HiVP MMIC

Bias @ 20V/550mA

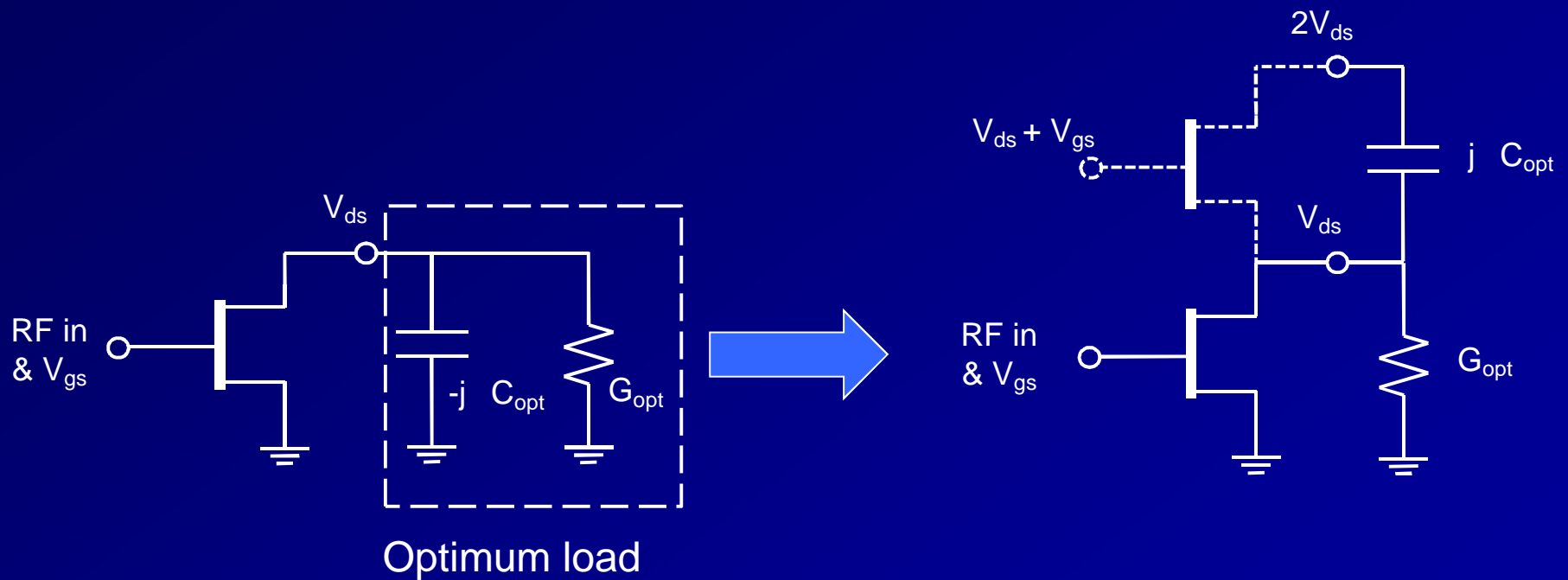


# UHiFET Concept

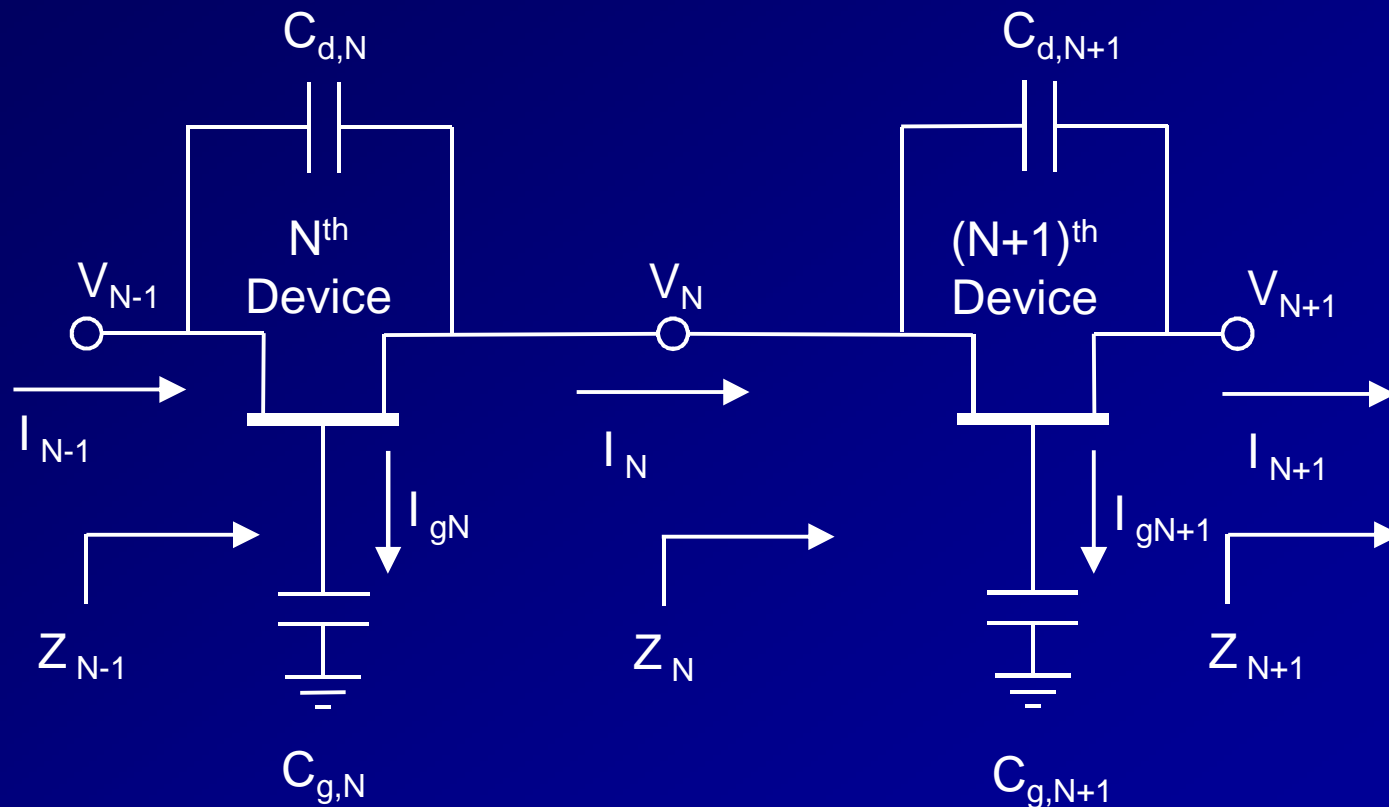
# New Universal High Voltage FET (UHiFET)



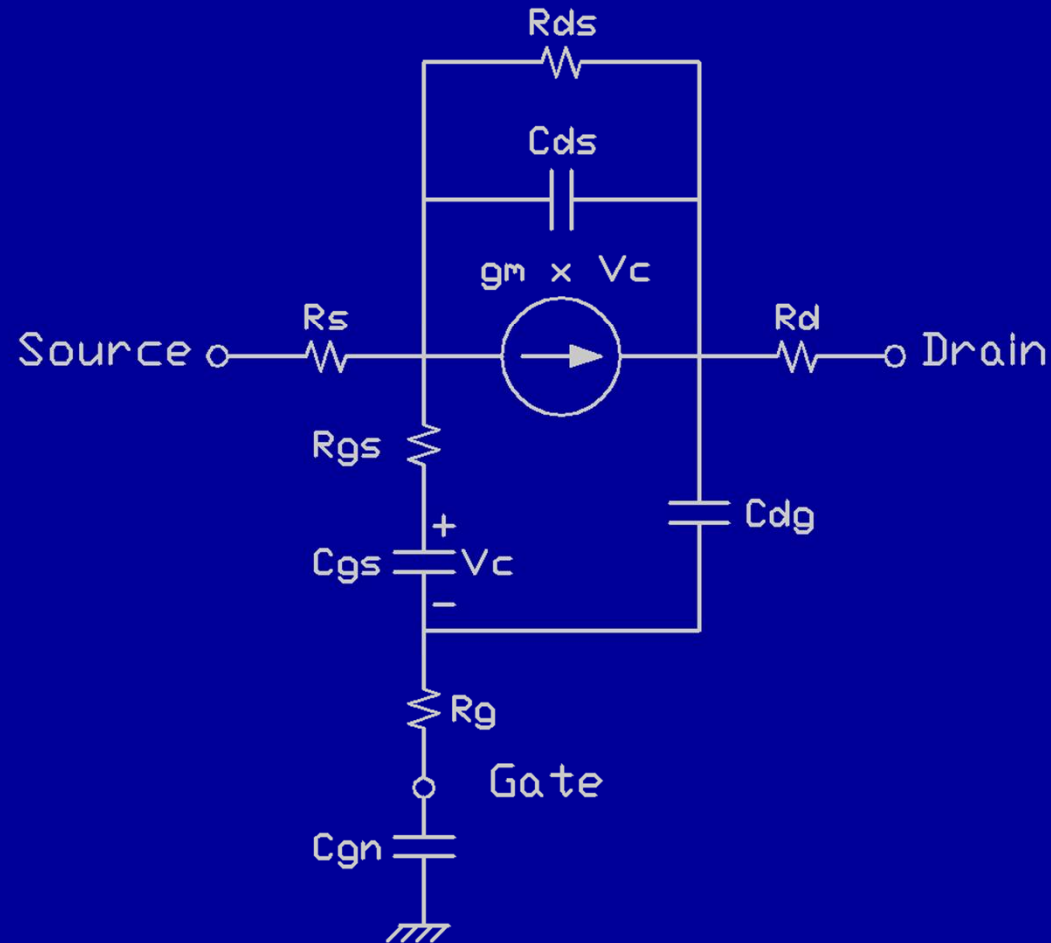
# Compensation Mechanism



# Cascaded Elements of the UHiFET



# Device RF Equivalent Circuit

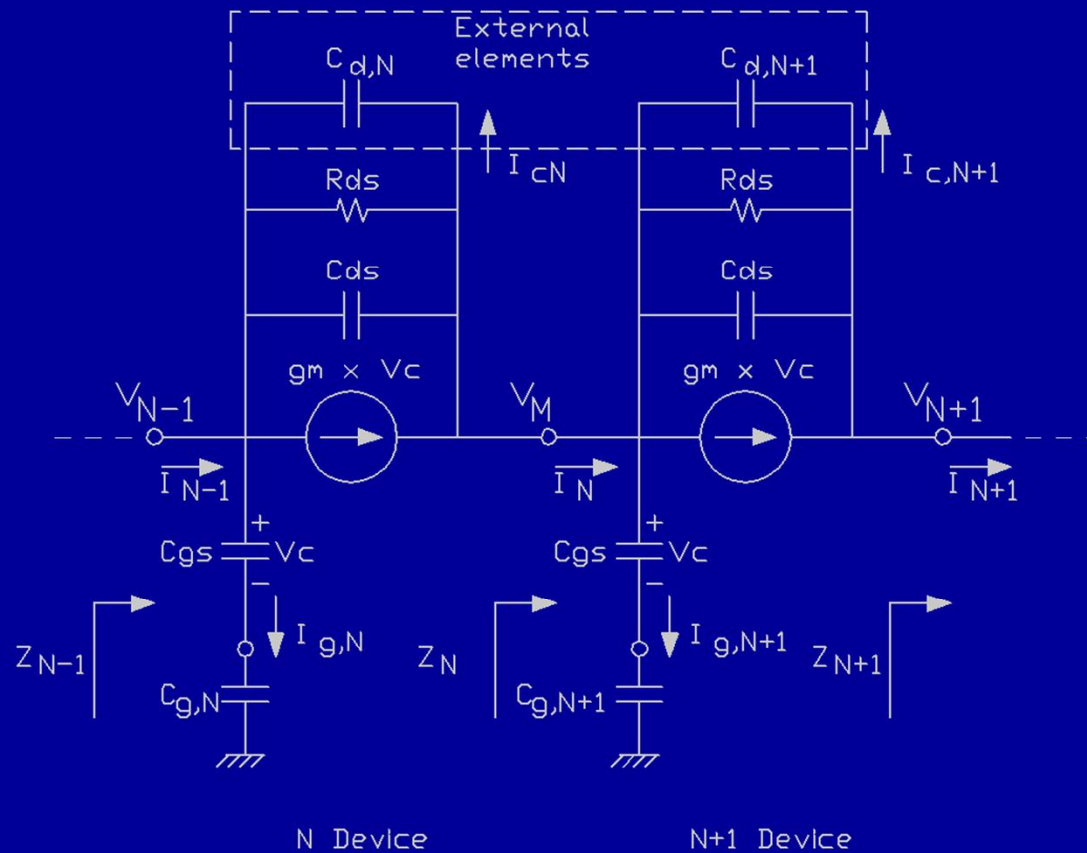


$$I_m = g_m V_c = g_m \frac{(N-1)V_m}{1 + \frac{C_{gs}}{C_{g,N}}}$$

# UHiFET Equivalent Circuit

$$V_{N+1} - V_N = V_N - V_{N-1} = V_m$$

$$I_m = g_m V_c = g_m \frac{(N-1)V_m}{1 + \frac{C_{gs}}{C_{g,N}}}$$



# Theoretical Derivation

$$C_{g,N} = \frac{C_{gs}}{g_m(N-1)/(G_{opt} - j\omega C_{opt} + j\omega C_{ds}) - 1}$$
$$\approx \frac{C_{gs}}{g_m(N-1)/G_{opt} - 1}$$

$$Y_{opt} = G_{opt} - j\omega C_{opt} \quad (\text{FET optimum load})$$

$$C_{d,N+1} \approx C_{d,N} + C_{gs} G_{opt} / g_m$$

Since  $C_{d,1} = 0$

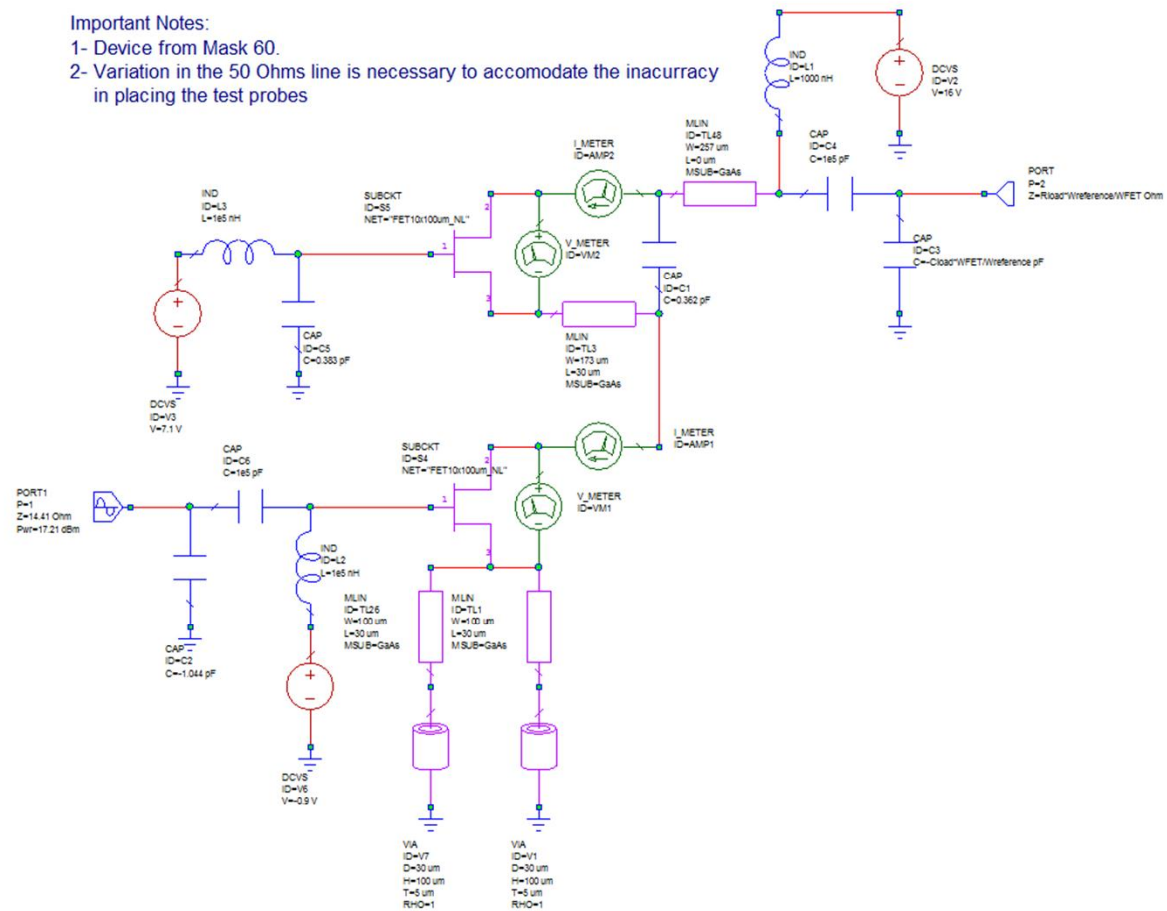
$$C_{d,N+1} \approx \frac{C_{gs}}{g_m} N G_{opt}$$

$$Y_N \approx \frac{Y_{opt} - j\omega C_{d,N}}{N} \approx \frac{Y_{opt}}{N} - \frac{j\omega C_{gs} (N-1) G_{opt}}{N g_m}$$

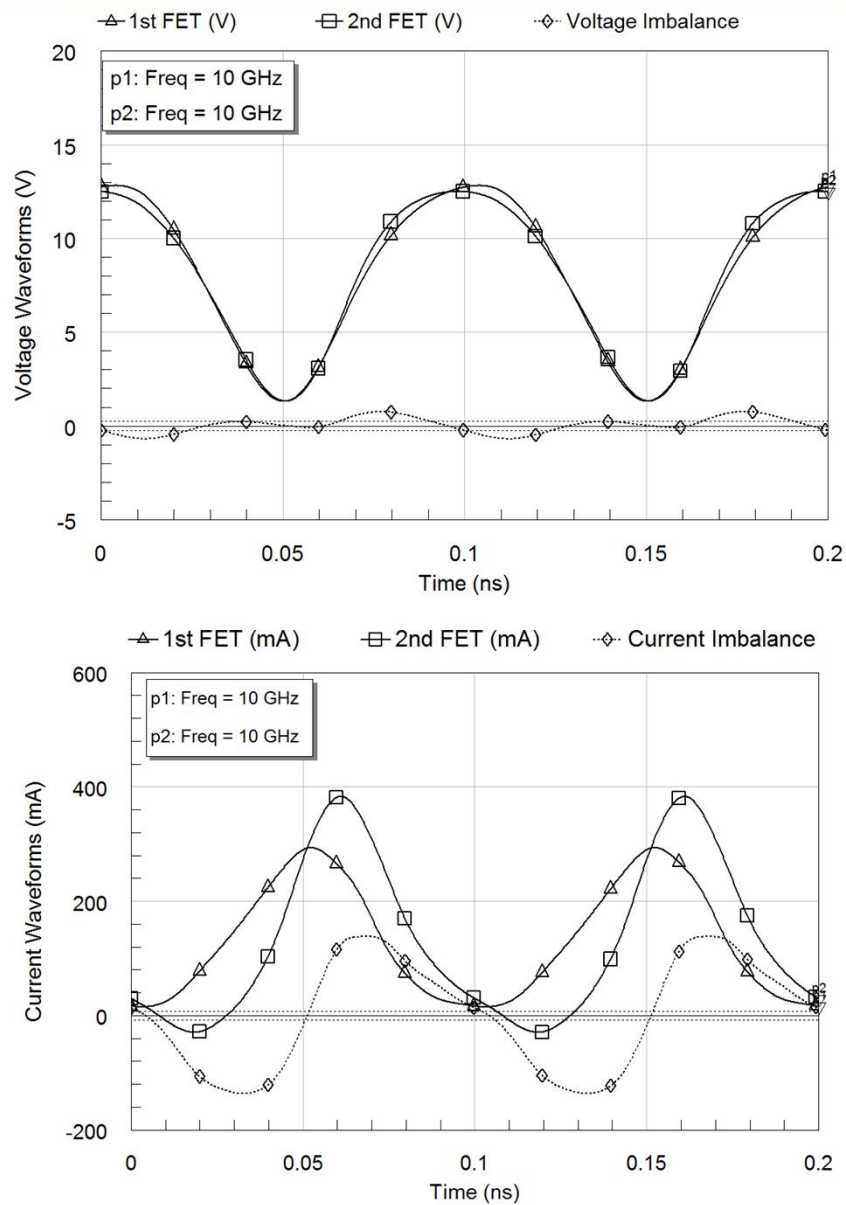
# 2 x 1 mm UHiFET Model

## Important Notes:

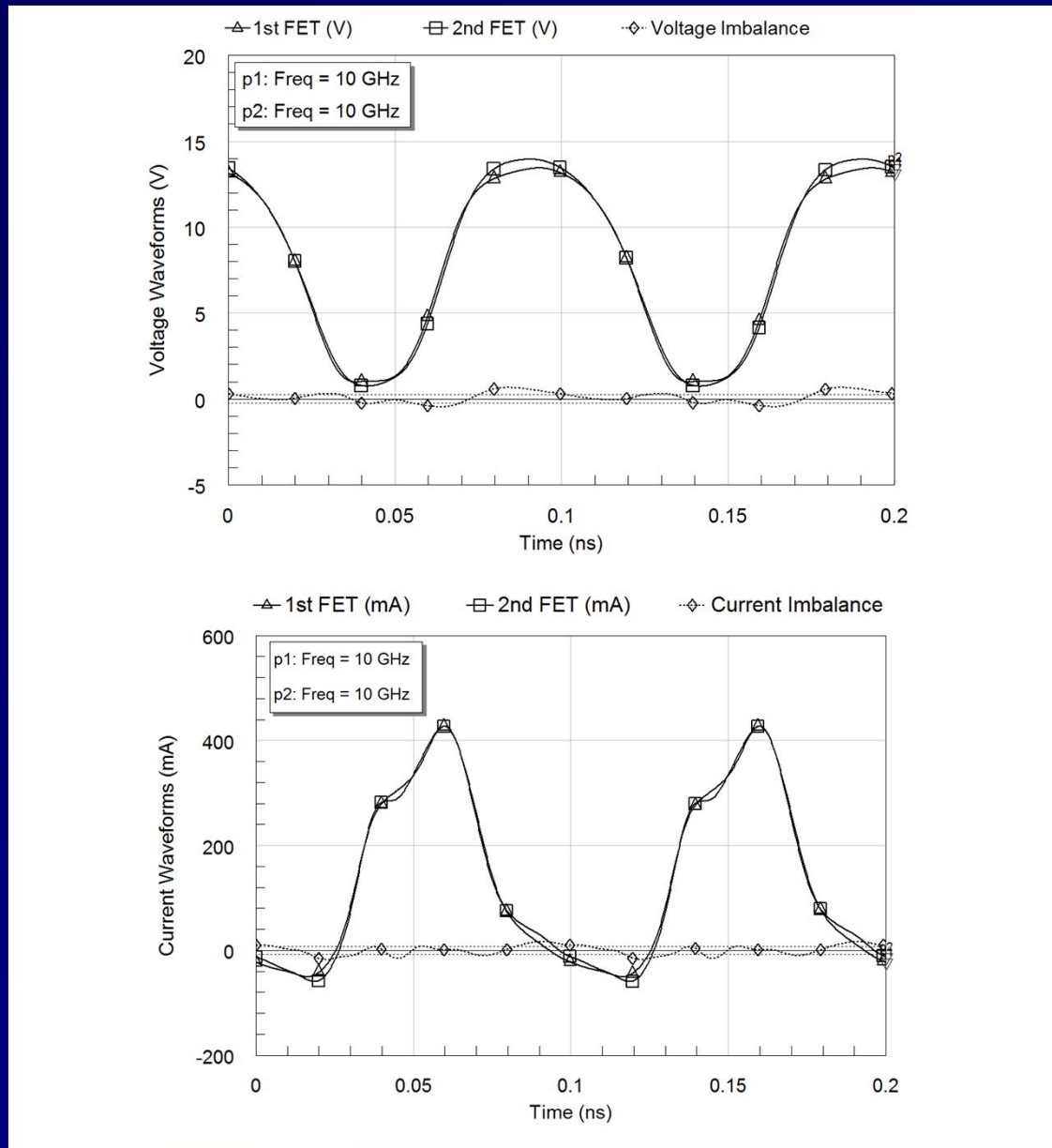
- 1- Device from Mask 60.
- 2- Variation in the 50 Ohms line is necessary to accommodate the inaccuracy in placing the test probes



# Optimized 2 x1mm HiVP



# Optimized 2x1mm UHiFET

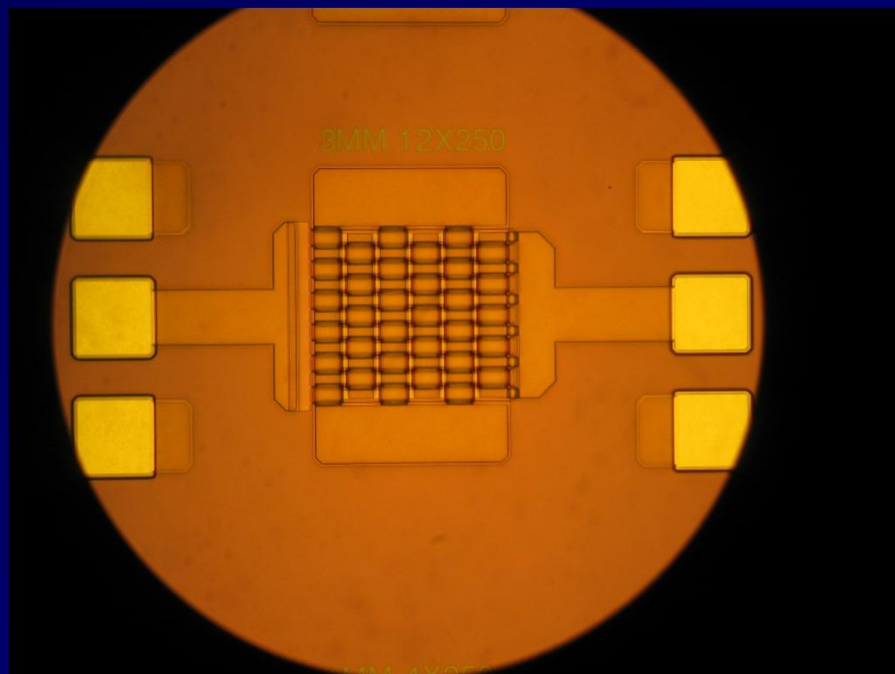


# Measurement Results

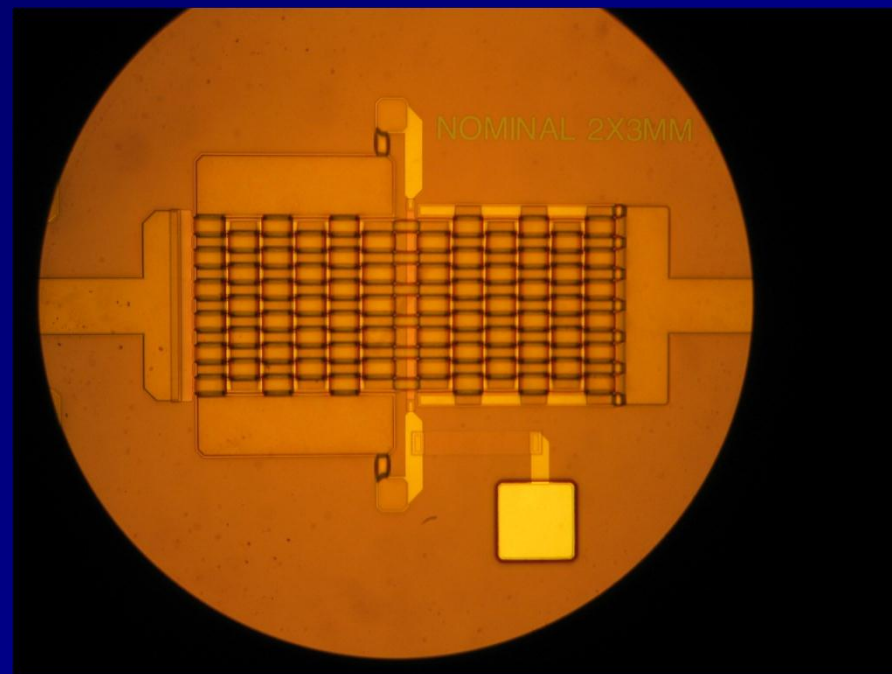
# Test Patterns

- Comparison made between 3 devices:
  - 3mm regular FET
  - 2 x 3mm Old HiVP
  - 2 x 3mm UHiFET
- Process is 0.5 $\mu$ m WIN pHEMT (0.6W/mm)
- Power and Efficiency measured at 7GHz

# Test Patterns

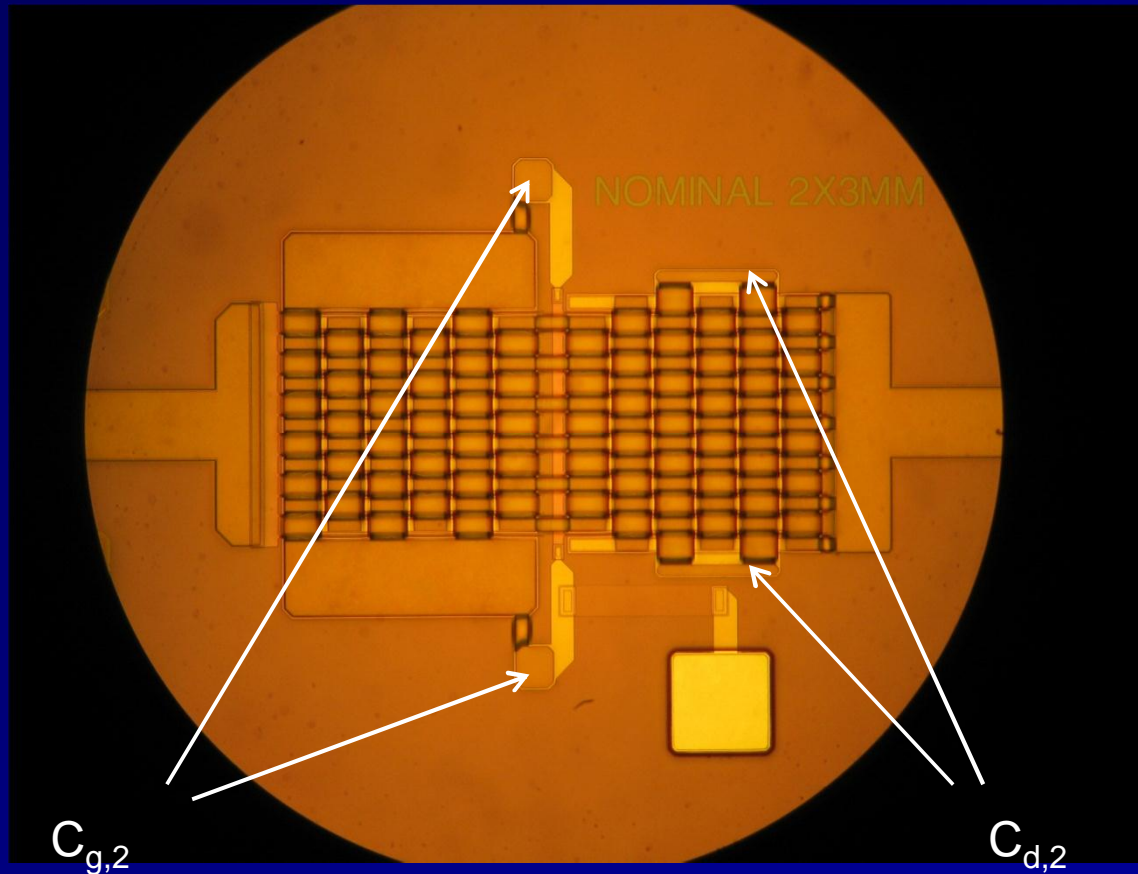


3mm FET (12 x 250 $\mu$ m)



2 x 3mm HiVP (2 x 12 x 250 $\mu$ m)

# Test Patterns

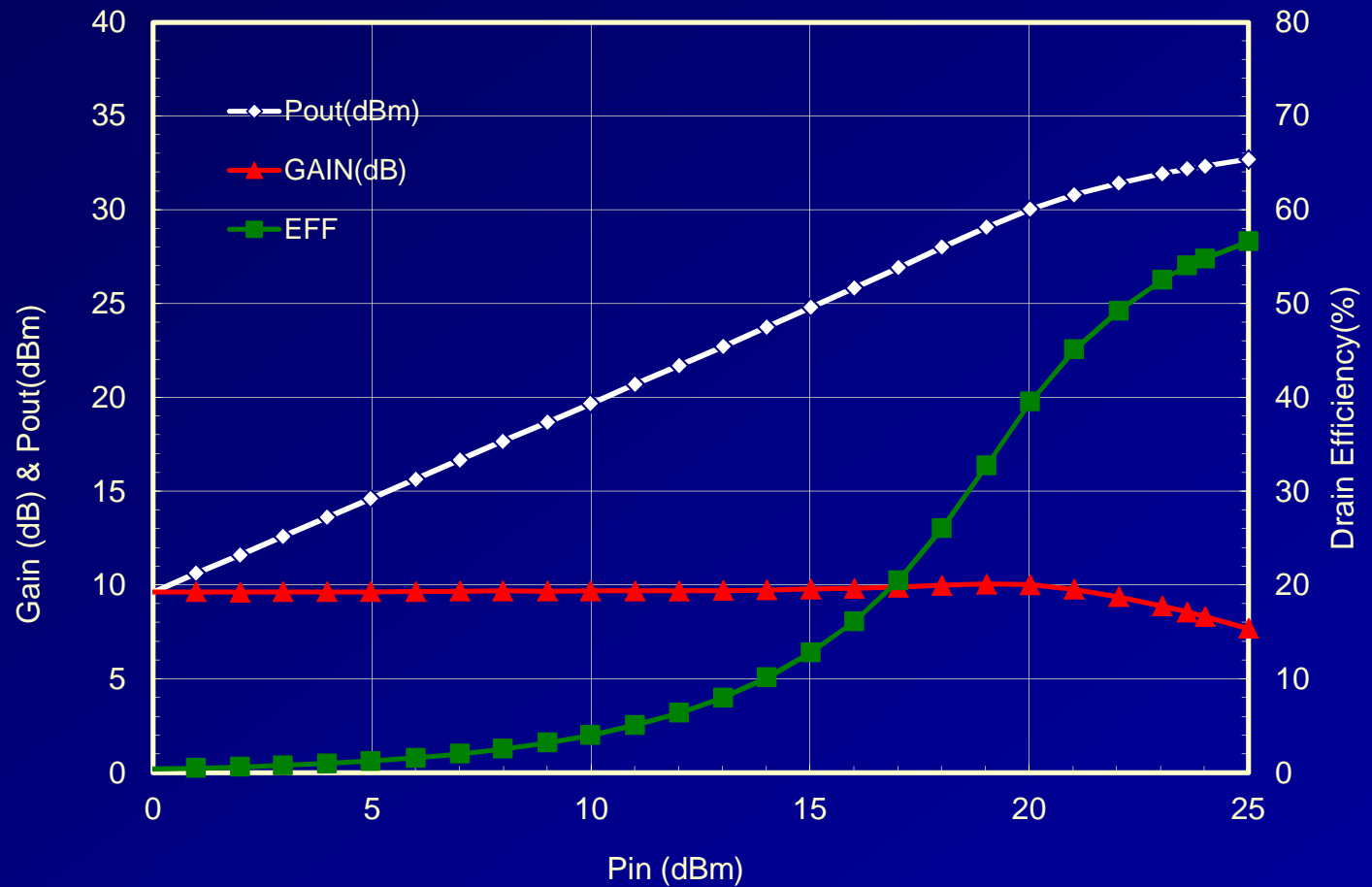


2x3mm UHFET (2 x 12 x 250 $\mu$ m)

# Power of a Single 3mm Device

$P_{1dB} = 32.0\text{dBm}$   
 $1\text{dB} = 50\%$   
 $G_{ss} = 10\text{dB}$

$P_{\text{max}} = 32.5\text{dBm}$   
 $\text{max} = 56\%$

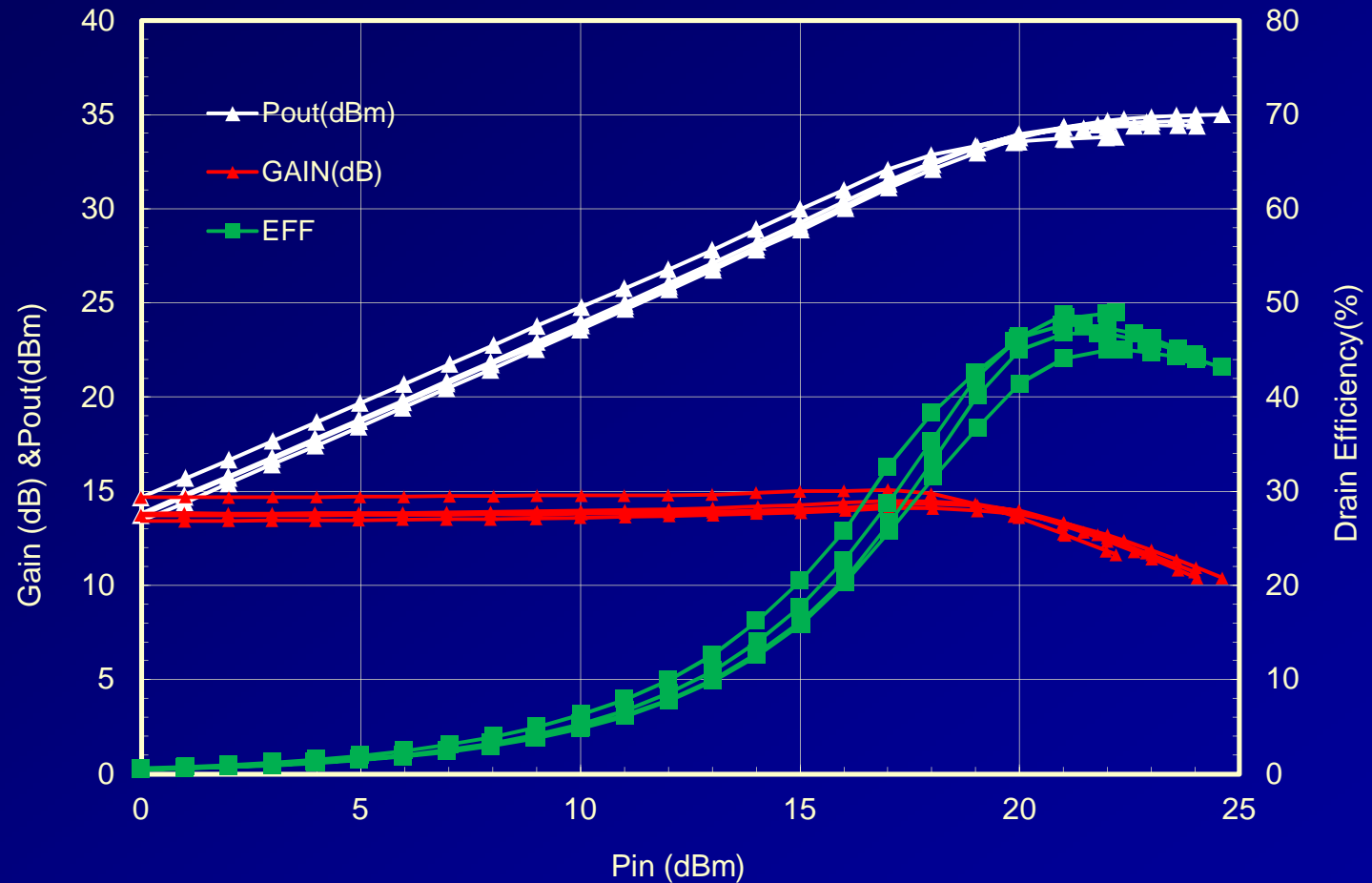


Performance of a single 3mm pHEMT @7GHz  
( $V_{dd} = +8\text{V}$ ,  $V_{gs} = -0.95\text{V}$ ,  $I_d = 0.4\text{A}$ )

# Power of a 2 x 3mm HiVP

$P_{1dB} = 34\text{dBm}$   
 $1\text{dB} = 48\%$   
 $G_{ss} = 14\text{dB}$

$P_{max} = 34.5\text{dBm}$   
 $max = 43\%$

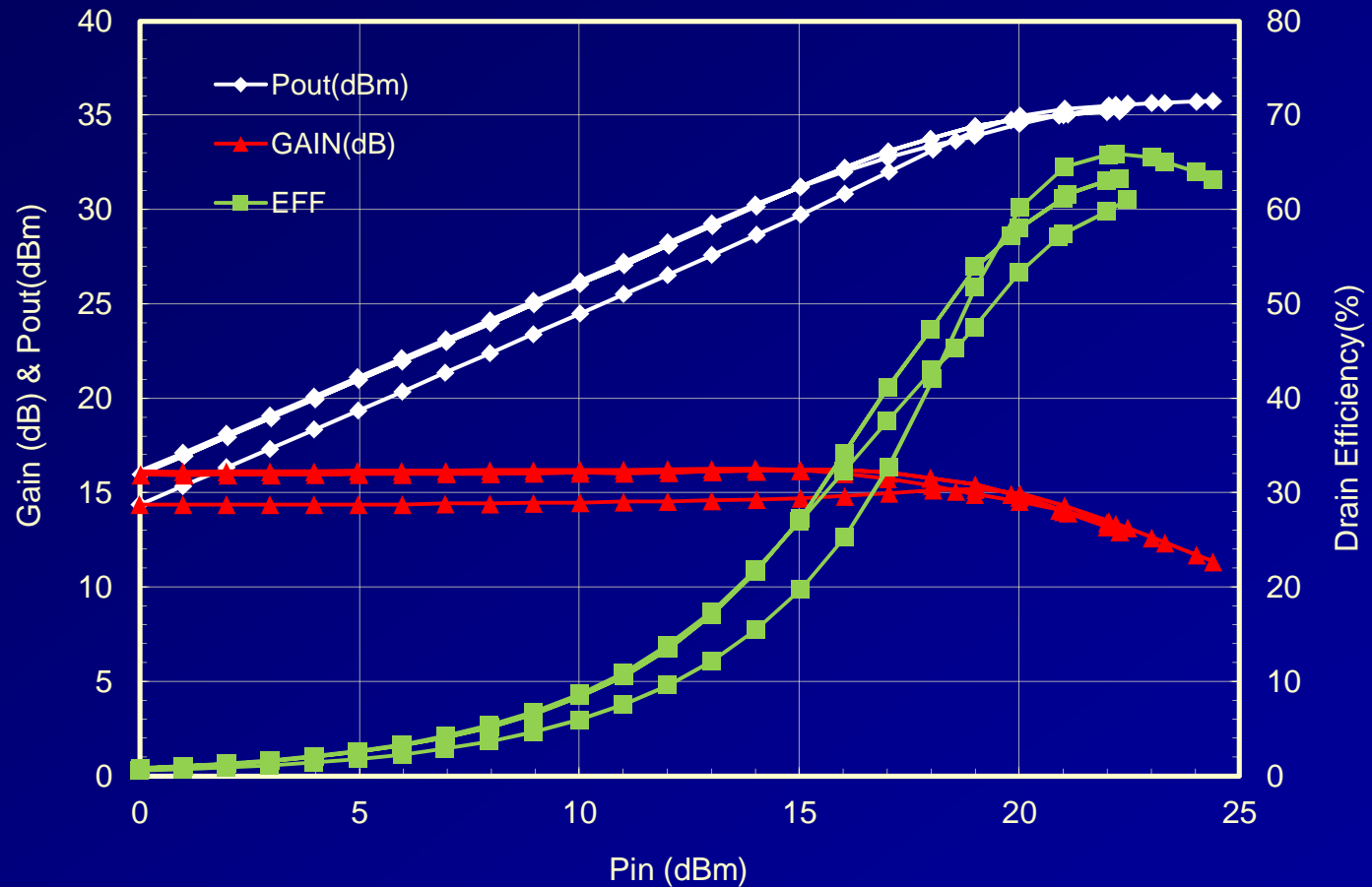


Performance of uncompensated 2x3mm HiFET @7GHz  
( $V_{dd} = +16\text{V}$ ,  $V_{gs} = -0.95\text{V}$ ,  $I_d = 0.4\text{A}$ )

# Power of a 2 x 3mm UHiFET

$P_{1dB} = 35\text{dBm}$   
 $1dB = 60\%$   
 $G_{ss} = 15\text{dB}$

$P_{max} = 36\text{dBm}$   
 $max = 63\%$



Performance of compensated 2 x 3 mm UHiFET @7GHz  
( $V_{dd} = +16\text{V}$ ,  $V_{gs} = -0.95\text{V}$ ,  $I_d = 0.4\text{A}$ )

# Comparison Table

| Configuration               | 3mm FET | 2 x 3mm HiVP | 2 x 3mm UHiFET |
|-----------------------------|---------|--------------|----------------|
| Gain                        | 9.5dB   | 15dB         | 15dB           |
| P1dB                        | 32dBm   | 34dBm        | 35dBm          |
| Efficiency@P <sub>1dB</sub> | 50%     | 48%          | 60%            |
| V <sub>dd</sub>             | +8V     | +16V         | +16V           |
| I <sub>dd</sub>             | 0.4A    | 0.4A         | 0.4A           |

# Conclusion

- An improvement to the original High Voltage FET configuration is presented
- This new UHiFET uses additional compensation elements to perfectly synchronize all series FETs
- This new configuration leads to perfect power combining and excellent efficiency
- The compensating technique used in the UHiFET is suitable for any frequency up to millimeter-wave frequencies