

## DESCRIPTION

AMCOM's AM012535MM-BM/FM-R is part of the GaAs MMIC power amplifier series. It has 20dB gain and 33dBm output power over most of the 0.03 to 2.5GHz band. This MMIC is in a ceramic package with both RF and DC leads at the lower level of the package to facilitate low-cost SMT assembly to the PC board. When mounting directly to PCB, please see application note AN700 for instructions. Because of high DC power dissipation, we strongly recommend to mount these devices directly on a metal heat sink. The AM012535MM-FM-R is the AM012535MM-BM-R mounted on a gold plated copper flange carrier. There are two screw holes on the flange to facilitate screwing on to a metal heat sink. This MMIC is RoHS compliant. This product is normally biased at 20V, but it works to as low as 6V with the same gain and reduced output power.

## FEATURES

- Wide bandwidth from 0.03 to 2.5GHz
- High output power, P<sub>1dB</sub> = 33dBm
- High gain, 20dB
- Input & output 50-ohm impedance

## APPLICATIONS

- Software Radio
- Instrumentation
- Gain block

## TYPICAL PERFORMANCE\*

(V<sub>dd</sub> = +20V, I<sub>dd1</sub> = 150mA, I<sub>dd2</sub> = 400mA, V<sub>gg1</sub> = -2.8V\*\*, V<sub>gg2</sub> = -0.9V\*\* T<sub>a</sub> = 25°C)

Parameters	Minimum	Typical	Maximum
Frequency	0.1 – 2.0GHz	0.03 – 2.5GHz	
Small Signal Gain	18dB	20dB	
Gain Ripple		± 1.0dB	± 2.0dB
P <sub>1dB</sub> (0.1 to 2GHz)	32.0dBm	33.0dBm	
P <sub>sat</sub> (0.1 to 2GHz)		33.5dBm	
Efficiency @ P <sub>1dB</sub>		20%	
IP3 @ 1GHz		45dBm	
Input Return Loss	10dB	15dB	
Output Return Loss	6dB	10dB	
Thermal Resistance		8°C/W	

\*Specifications subject to change without notice.

\*\* V<sub>gg1</sub> & V<sub>gg2</sub> may vary from lot to lot

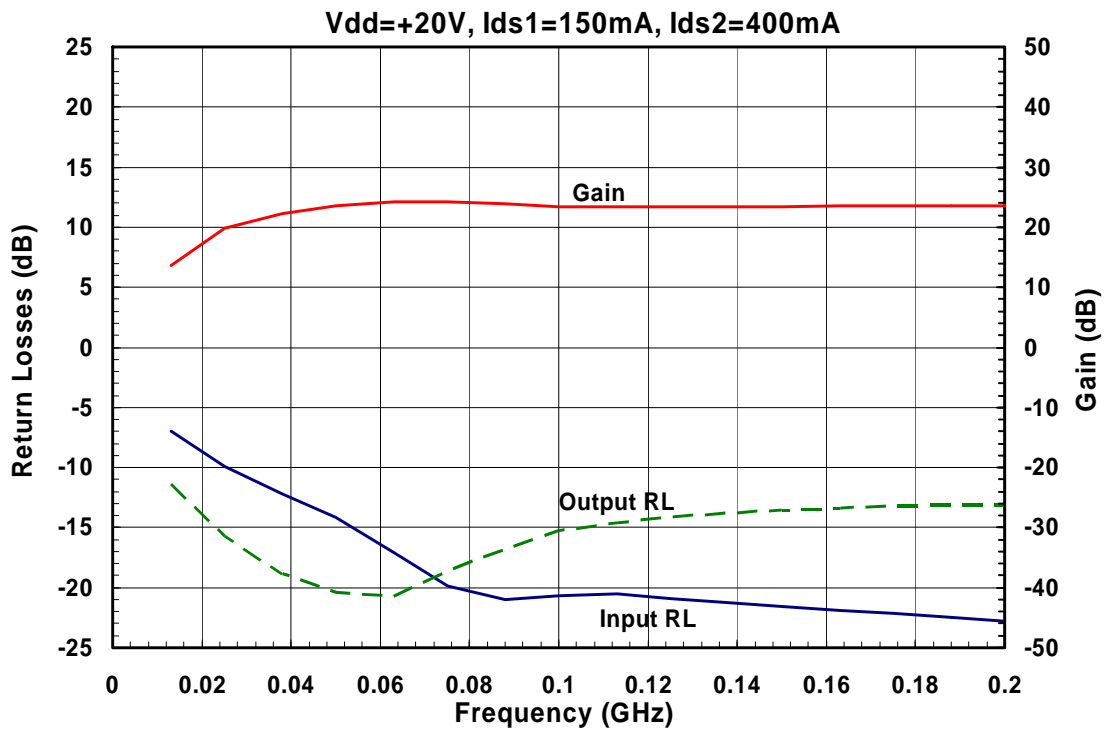
### Performance at low DC bias voltages

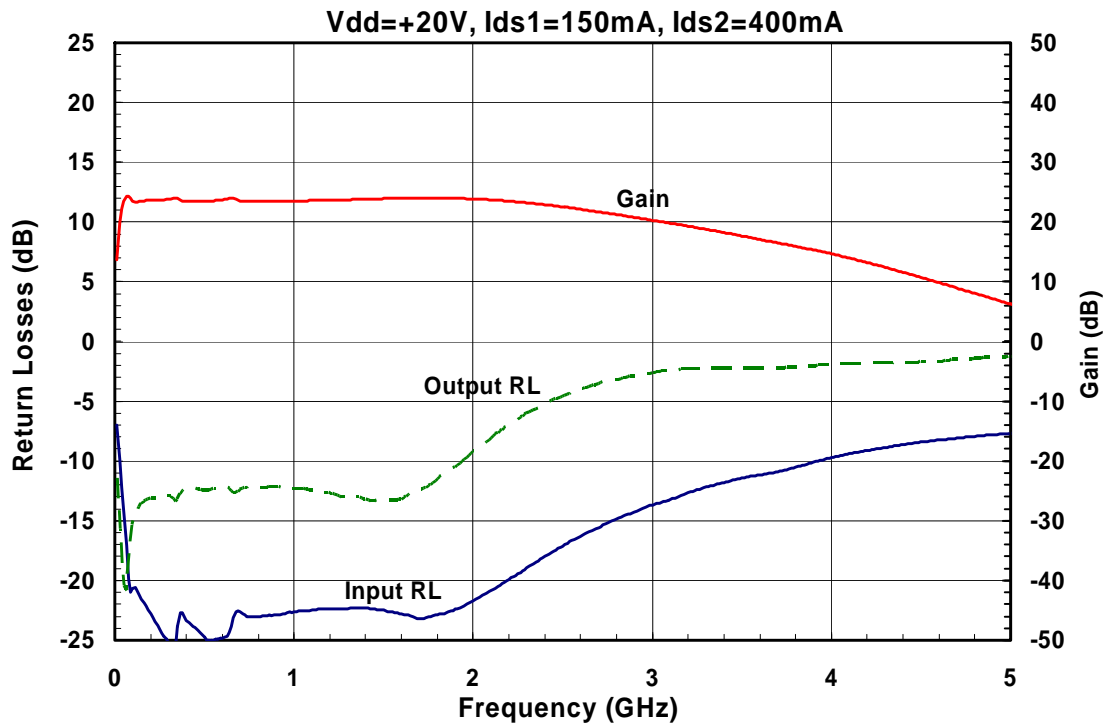
Drain source voltage	V <sub>ds</sub> = 6V	V <sub>ds</sub> = 8V	V <sub>ds</sub> = 10V
Frequency Band	0.03 – 2.5GHz	0.03-2.5GHz	0.03-2.5GHz
Small Signal Gain	22dB	22dB	22dB
Output Power P <sub>1dB</sub>	23.5dBm	24dBm	24.2dBm

**ABSOLUTE MAXIMUM RATING**

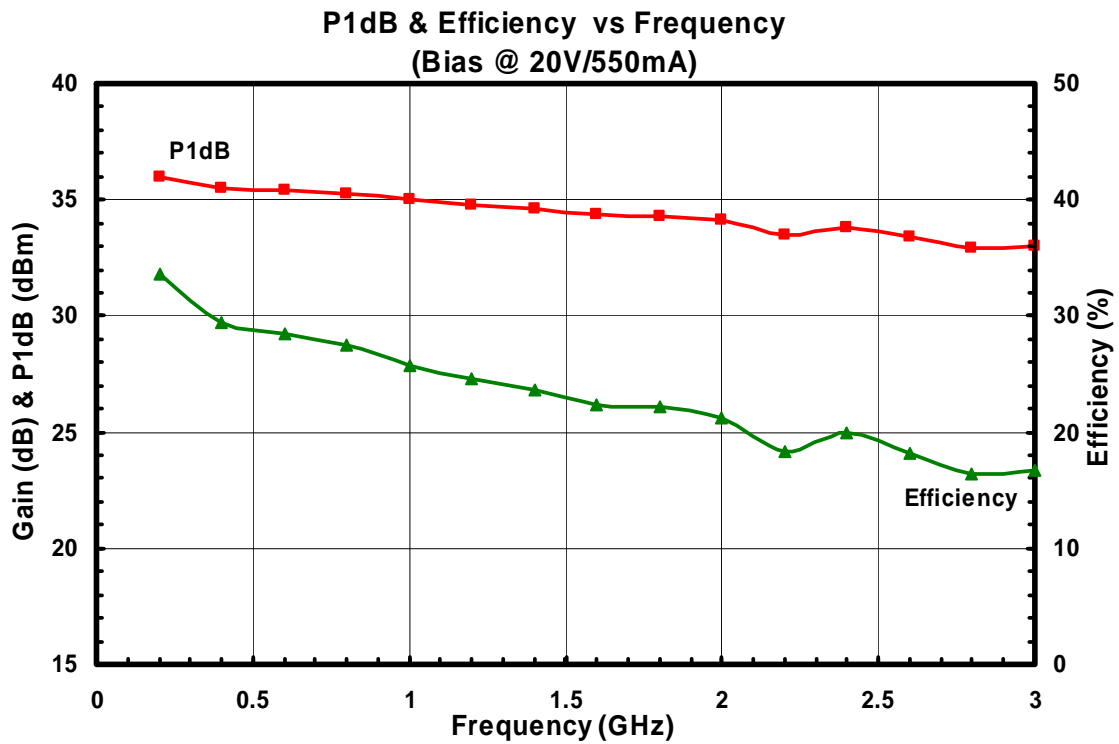
Parameters	Symbol	Rating
Drain source voltage	$V_{dd}$	24V
Gate source voltage	$V_{gg1}, V_{gg2}$	-8V
Drain source current	$I_{dd1} + I_{dd2}$	0.8A
Continuous dissipation at room temperature	$P_t$	18W
Channel temperature	$T_{ch}$	175°C
Storage temperature	$T_{sto}$	-55°C to +135°C

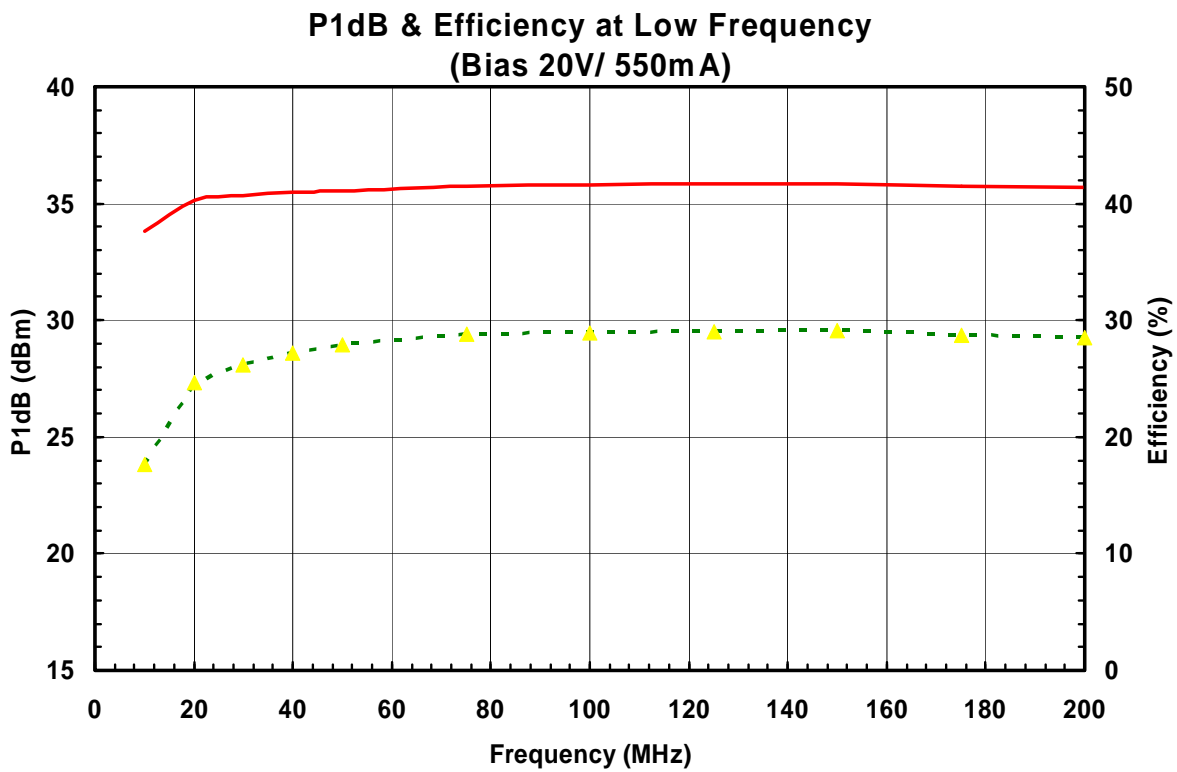
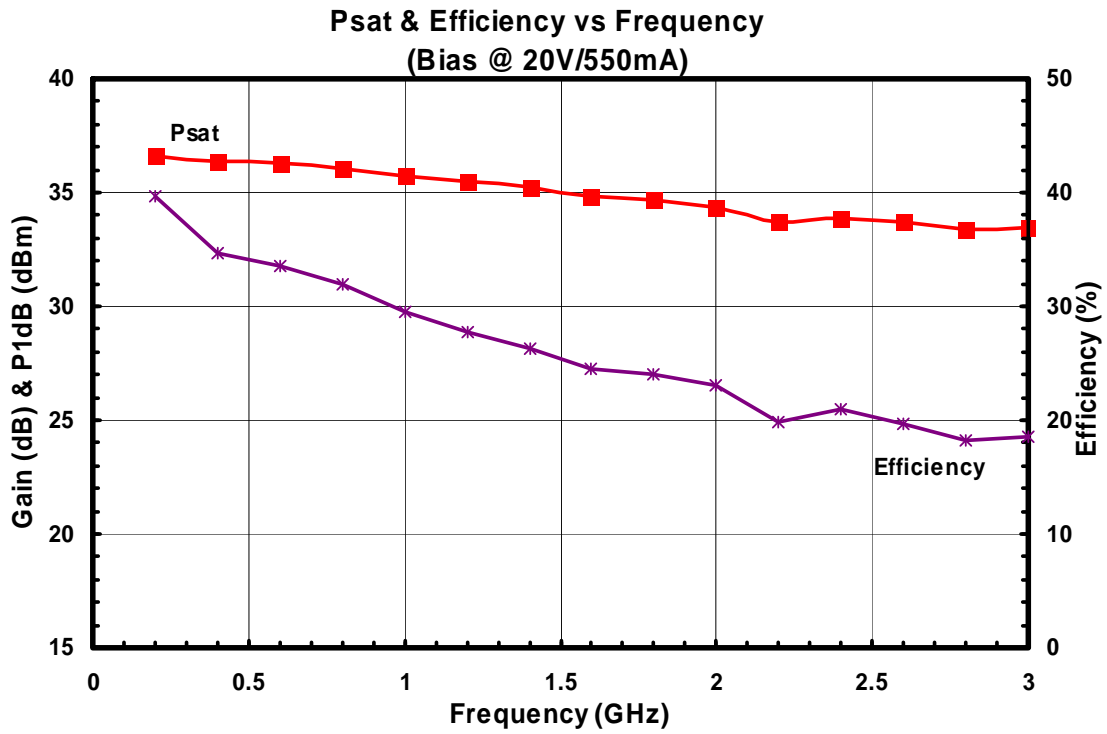
**SMALL SIGNAL DATA** (measurements performed with test fixture)

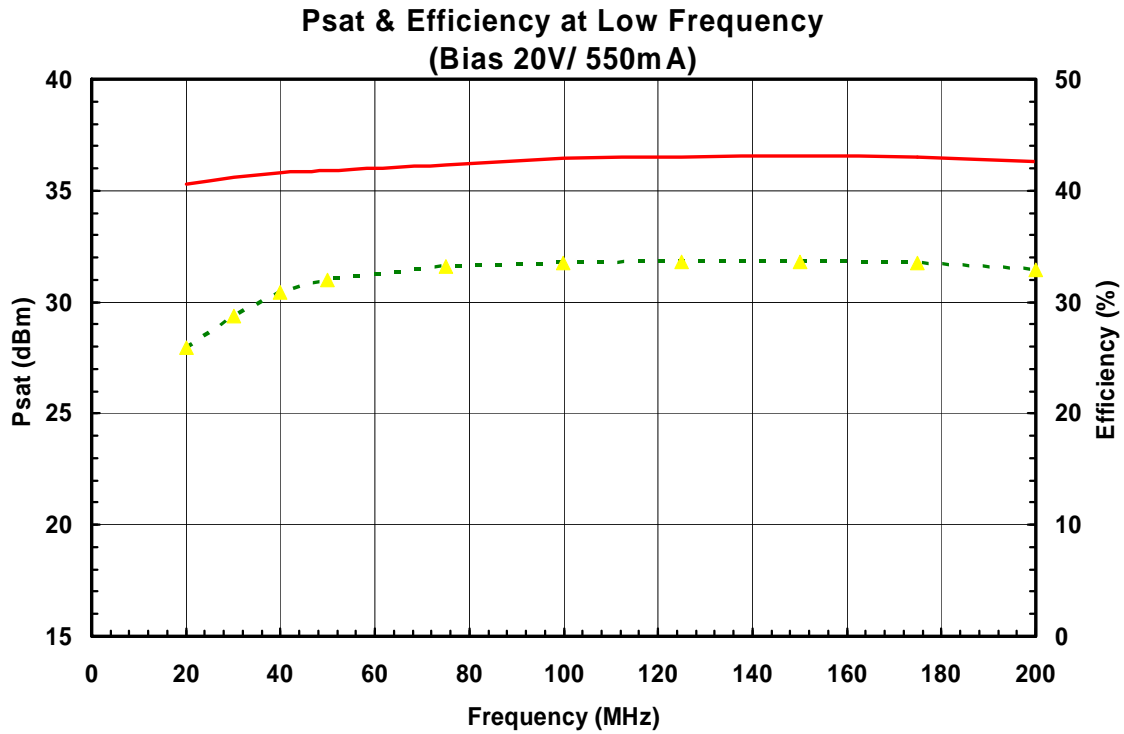




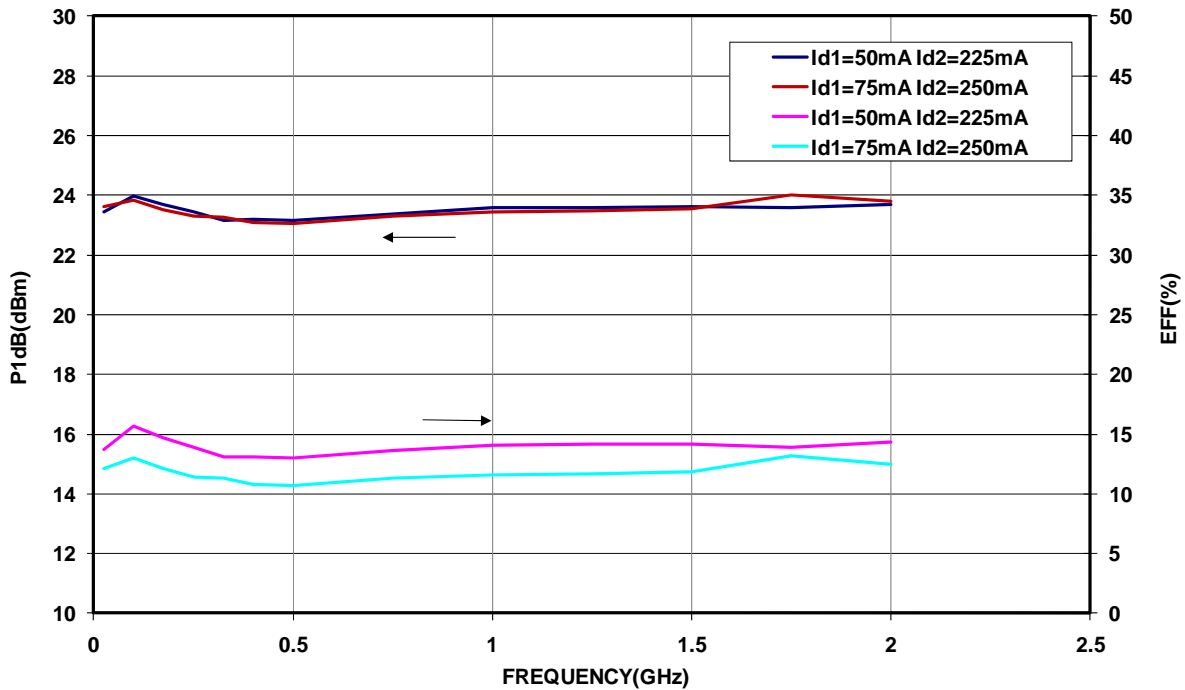
POWER DATA (Measurements performed with bias tee)



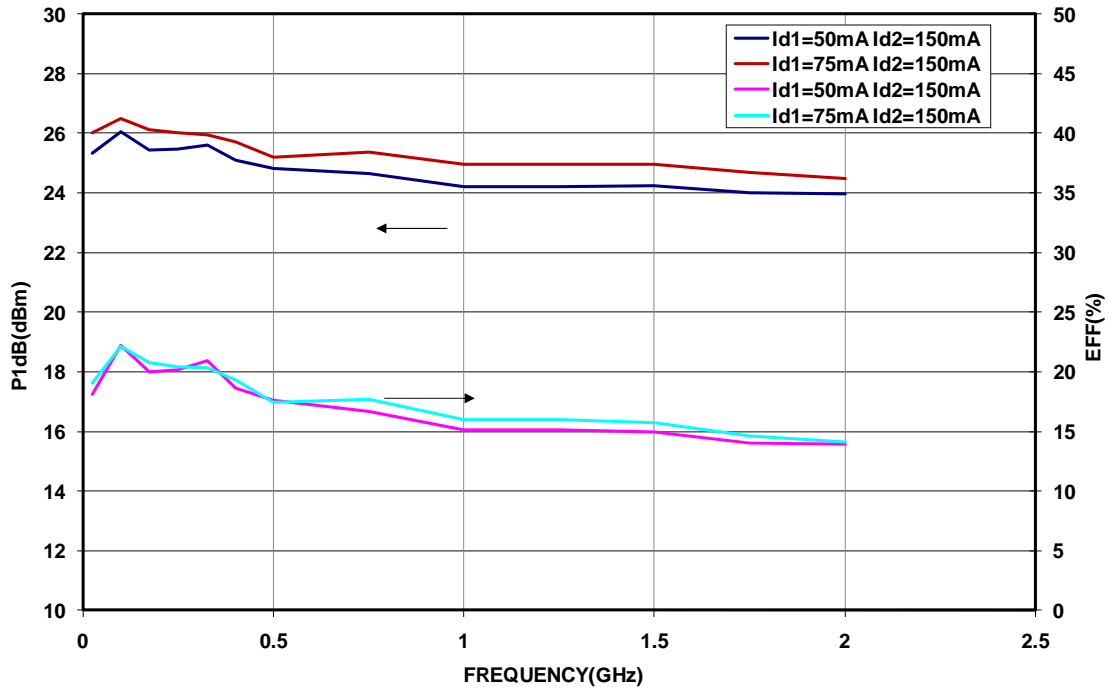




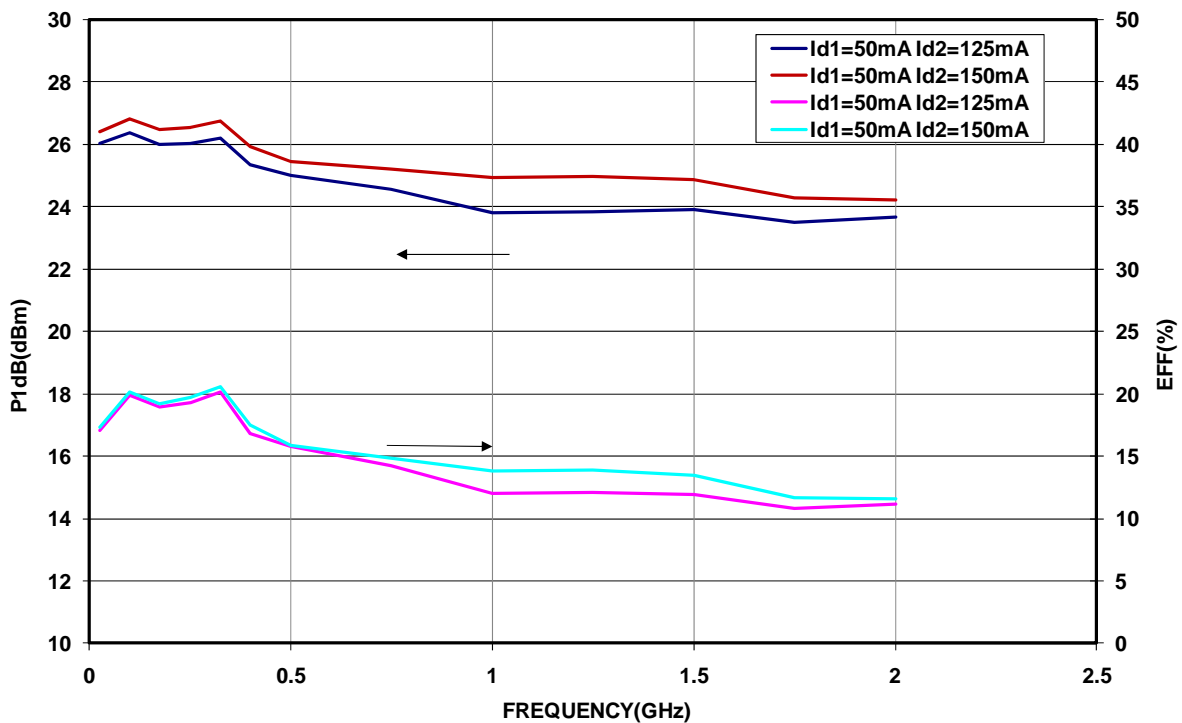
AM012535MM-BM-R  
Vds=6V



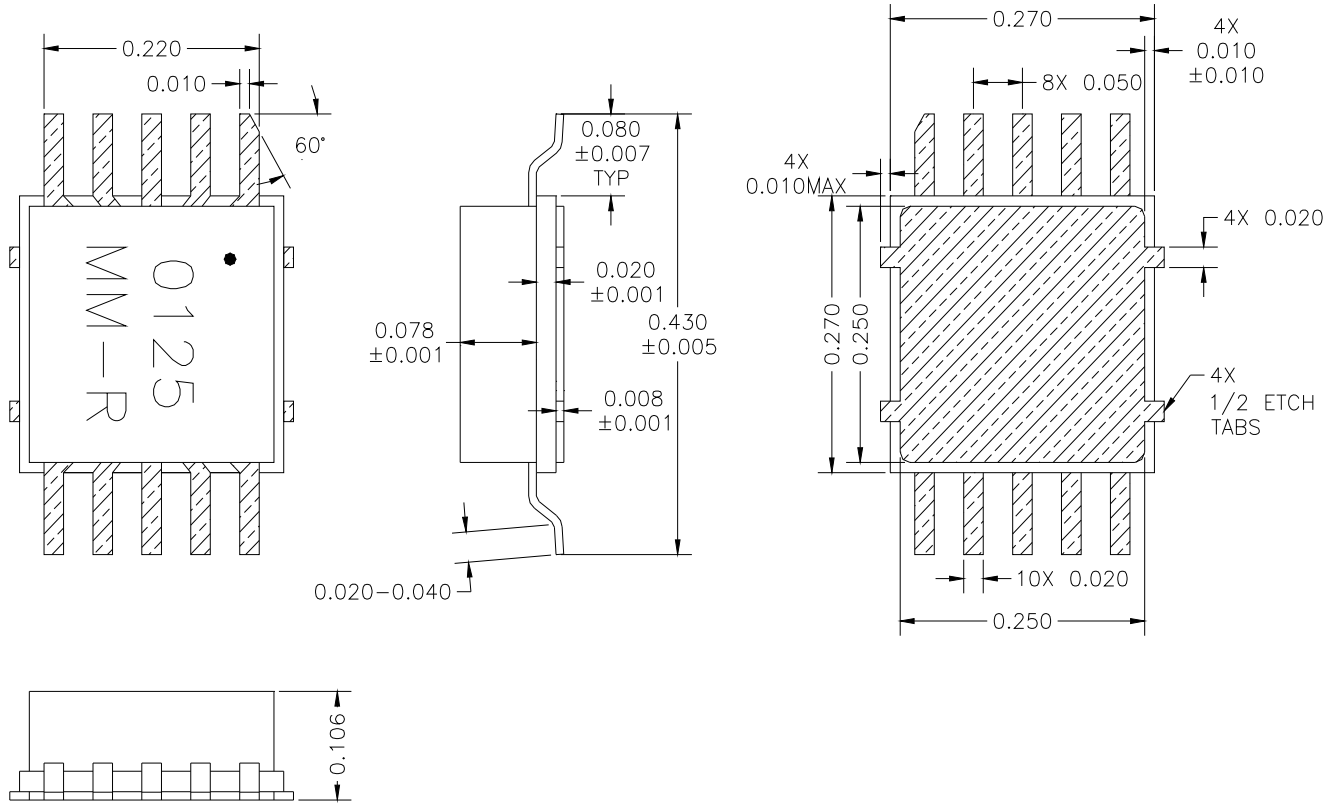
AM012535MM-BM-R  
 Vds=8V



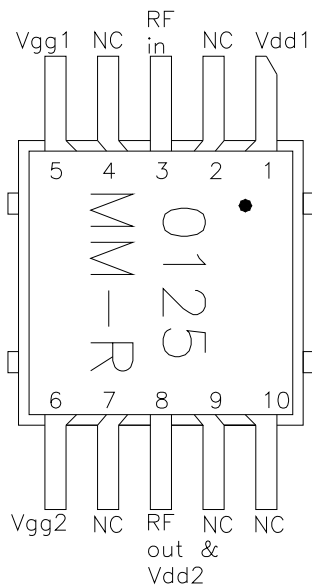
AM012535MM-BM-R  
 Vds=10V



PACKAGE OUTLINE (BM)



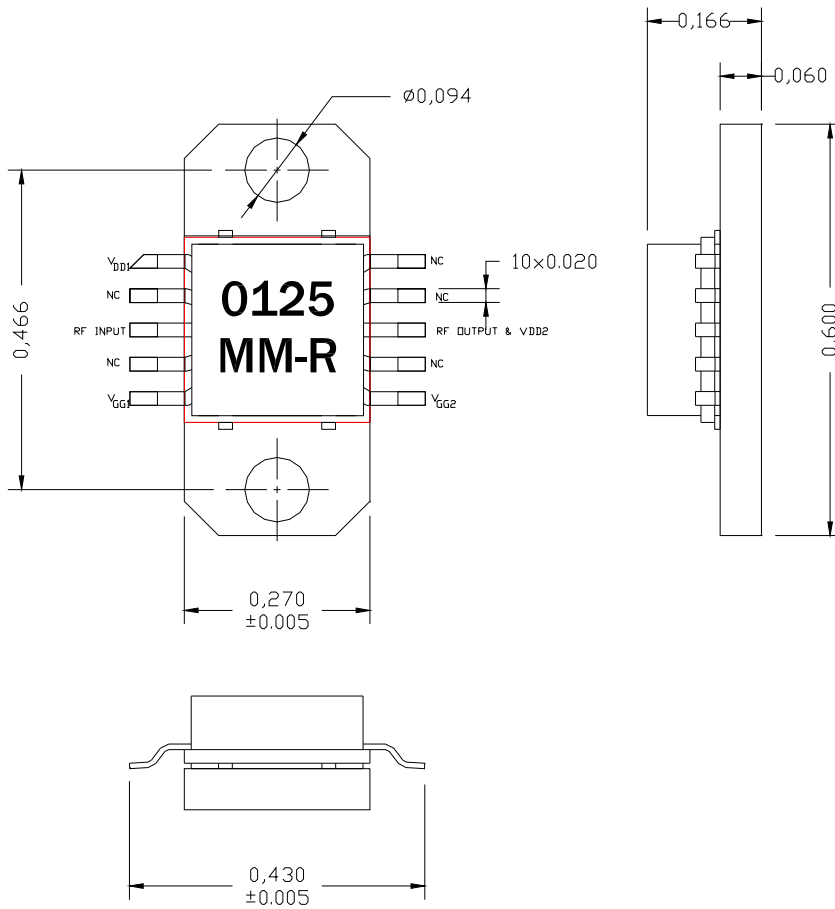
PIN LAYOUT



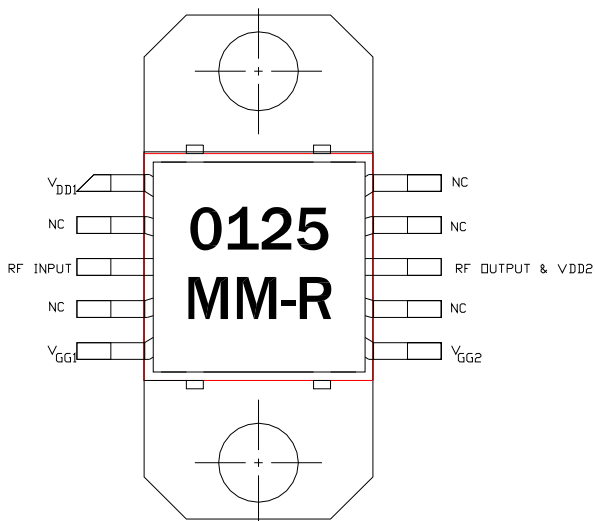
Pin No.	Function	Bias*
1	Vdd1	+20V
2	NC	
3	RF in	
4	NC	
5	Vgg1	-2.8V
6	Vgg2	-0.9V
7	NC	
8	RF out & Vdd2	+20V
9	NC	
10	NC	

\* V<sub>gg1</sub> & V<sub>gg2</sub> may vary from lot to lot

PACKAGE OUTLINE (FM)



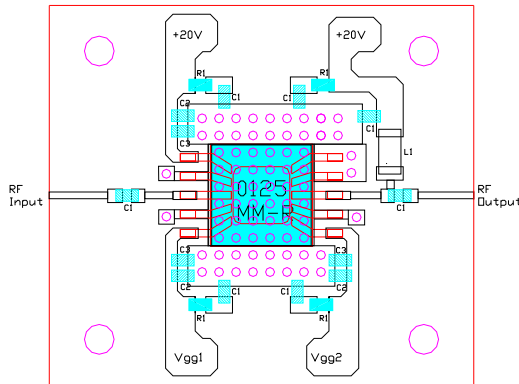
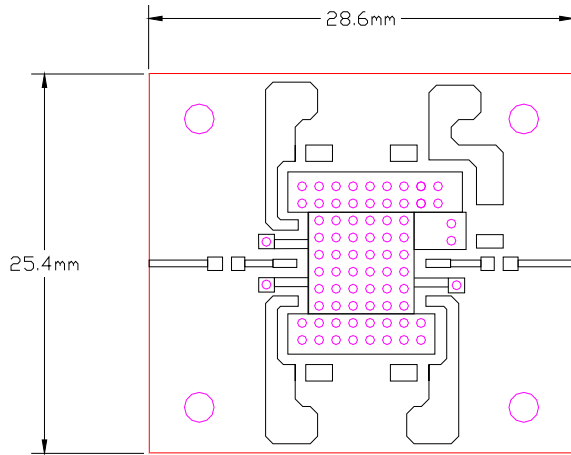
PIN LAYOUT



Pin No.	Function	Bias*
1	Vdd1	+20V
2	NC	
3	RF in	
4	NC	
5	Vgg1	-2.8V
6	Vgg2	-0.9V
7	NC	
8	RF out & Vdd2	+20V
9	NC	
10	NC	

\* V<sub>gg1</sub> & V<sub>gg2</sub> may vary from lot to lot

TEST CIRCUIT (BM)



Notes:

- 1- Material is 10mils FR4 with 1 Oz Copper
- 2- All vias are plated thru (min. via thickness = 25um)
- 3- R1=50Ohms, R2=0Ohms, C1=1000pF, C2=100pF, C3=20pF, L1=300nH
- 4- Bias could be supplied to the RF output port using a bias tee.

IMPORTANT NOTES:

- 1- The +20V Bias to the output port could be provided via a bias tee or suitable chokes to be soldered on the board. Inductance of choke should be large enough to have high impedance at lowest frequency of operation (300nH is adequate).
- 2- Recommended current biases are 150mA and 400mA for the first stage and second stage respectively. At  $V_{dd1}$  &  $V_{dd2} = +20V$   $V_{gg1}$  &  $V_{gg2}$  values are around -2.8V and -0.9V respectively to obtain these desired currents but may vary from lot to lot.  $V_{gg1}$  &  $V_{gg2}$  could be adjusted to vary the currents going thru the first stage ( $V_{dd1}$  pin) and the second stage ( $V_{dd2}$  pin) respectively.
- 3- Do not apply  $V_{dd1}$  &  $V_{dd2}$  without proper negative voltages on  $V_{gg1}$  &  $V_{gg2}$ .
- 4- Due to direct DC connection between  $V_{dd1}$  &  $V_{gg1}$  pins through a large resistor there is a current around 10mA flowing out of the  $V_{gg1}$  pin. The current flowing out of the  $V_{gg2}$  pin is less than 100µA.
- 5- External 1 µF dipped tantalum capacitor should be attached to Vd and Vg to decouple external bias leads.