

DESCRIPTION

AMCOM's AM012020WM-BM-R is a broadband low noise power amplifier. It is part of the GaAs MMIC power amplifier series. It has 2dB Noise Figure, 30dB gain, and 17dBm output P1dB over a broadband of 0.1 to 2 GHz. This MMIC is in a ceramic package with both RF and DC leads at the bottom level of the package to facilitate low-cost SMT assembly to the PC board. It is RoHS compliant.

FEATURES

- Wide bandwidth 0.1 to 2 GHz
- Low noise performance
- 20dBm of saturated output power.
- High gain, 30dB
- Fully matched; 50-ohm input/output impedance

APPLICATIONS

- Instrumentation
- Cellular Bands
- Two way radio
- Broadband Receivers

PERFORMANCE* ($V_{d1\&2}=8V$, $I_{d1\&2} = 30mA, 50mA$, $V_{g1\&2}^{**} = -1.3, -1.15 V$ $T_a = 25^\circ C$)

| Parameters | Minimum | Typical | Maximum |
|--------------------------|-----------|---------------|--------------|
| Frequency | 0.2 – 1.8 | 0.1 – 2.0 GHz | |
| Gain (Small signal) | 28 dB | 30 dB | |
| Gain Ripple | | ± 1.0 dB | ± 3.0 dB |
| P_{1dB} | 15.0 dBm | 16.0 dBm | |
| P_{sat} | | 17.0 dBm | |
| Noise Figure @Pin=-20dBm | | 2.0dB | 3.0dB |
| Input Return Loss | -10 dB | -15 dB | |
| Output Return Loss | -8 dB | -10 dB | |
| Thermal Resistance | | 4.9 °C/W | |

* Specifications subject to change without notice

** Gate bias is for reference only and may vary from lot to lot

ABSOLUTE MAXIMUM RATING

| Parameter | Symbol | Rating |
|--|-----------|-----------------|
| Drain source voltage | V_{ds} | 15 V |
| Gate source voltage | V_{gs} | -5V or +0.5V |
| Drain source current | I_{ds} | .2 A |
| Continuous dissipation at room temperature | P_t | 3 W |
| Channel temperature | T_{ch} | 175 °C |
| Operating temperature | T_{op} | -55°C to +100°C |
| Storage temperature | T_{sto} | -55°C to +135°C |

SMALL SIGNAL DATA

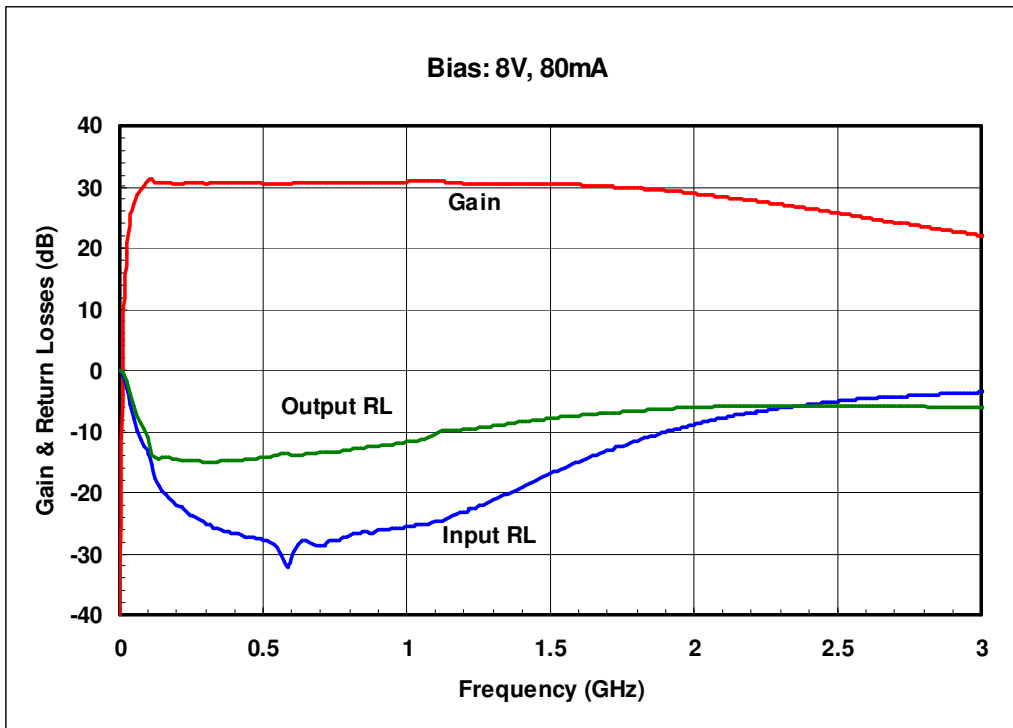


Figure1: Gain & Return Losses vs. Frequency

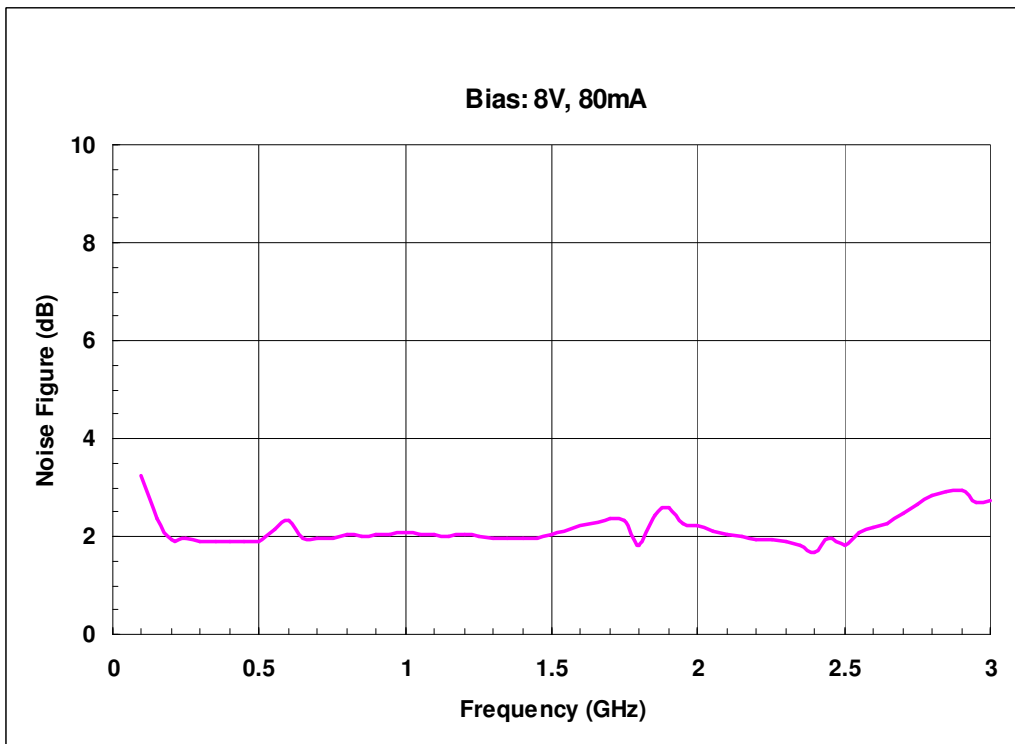


Figure2: Noise Figure vs. Frequency

POWER DATA

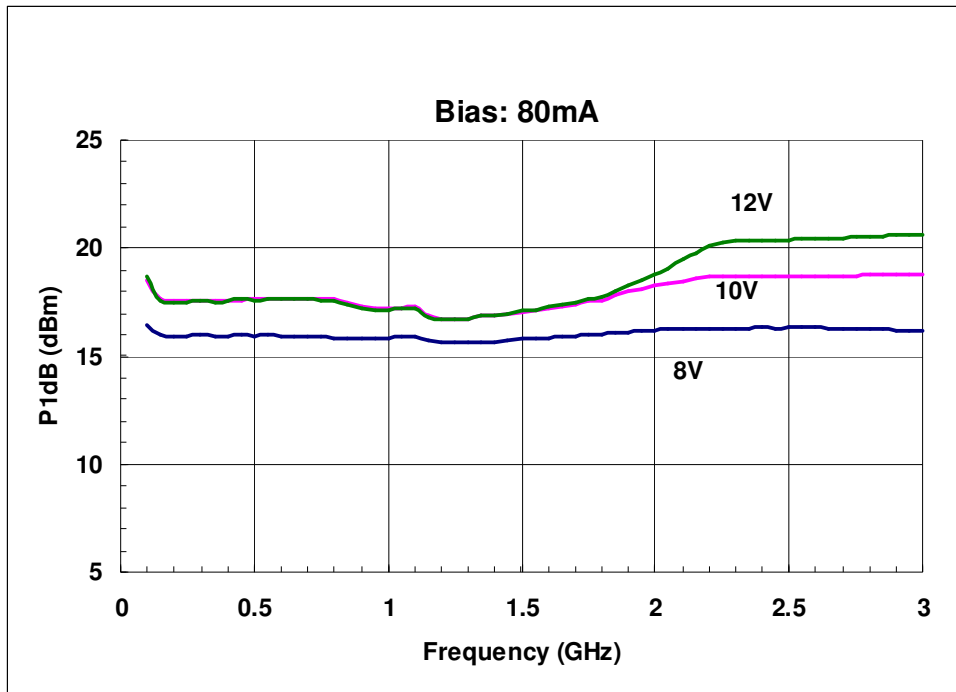


Figure3: P1dB vs. Frequency at different drain voltages

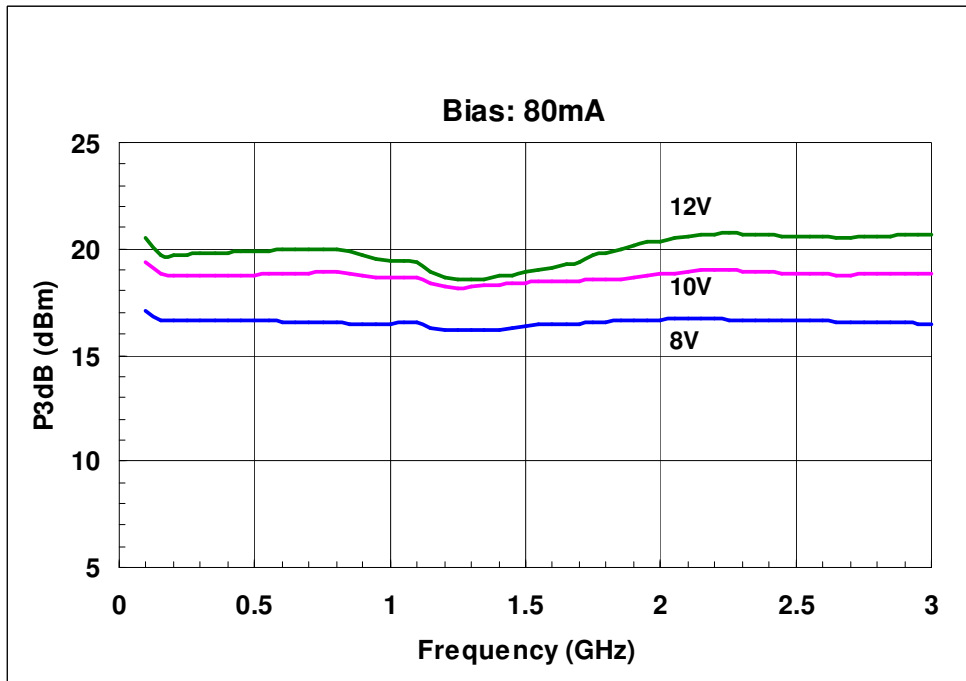


Figure4: P3dB vs. Frequency at different drain voltages

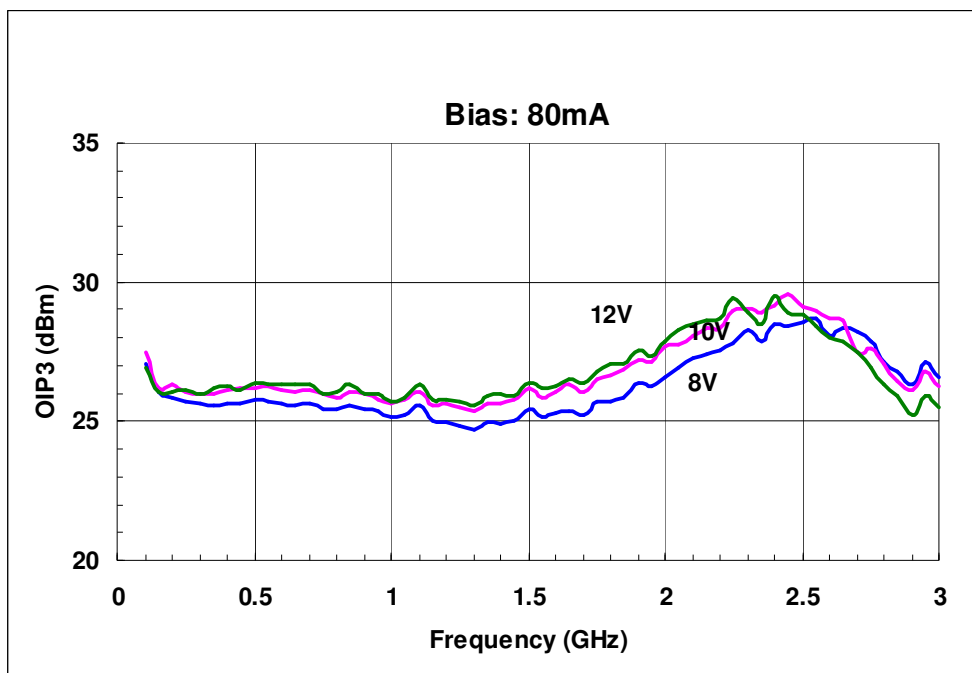
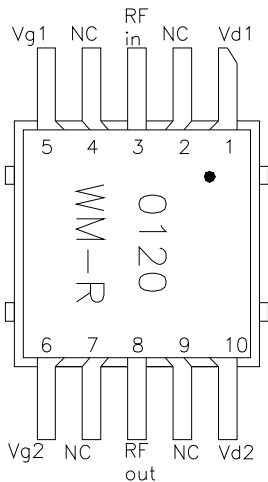
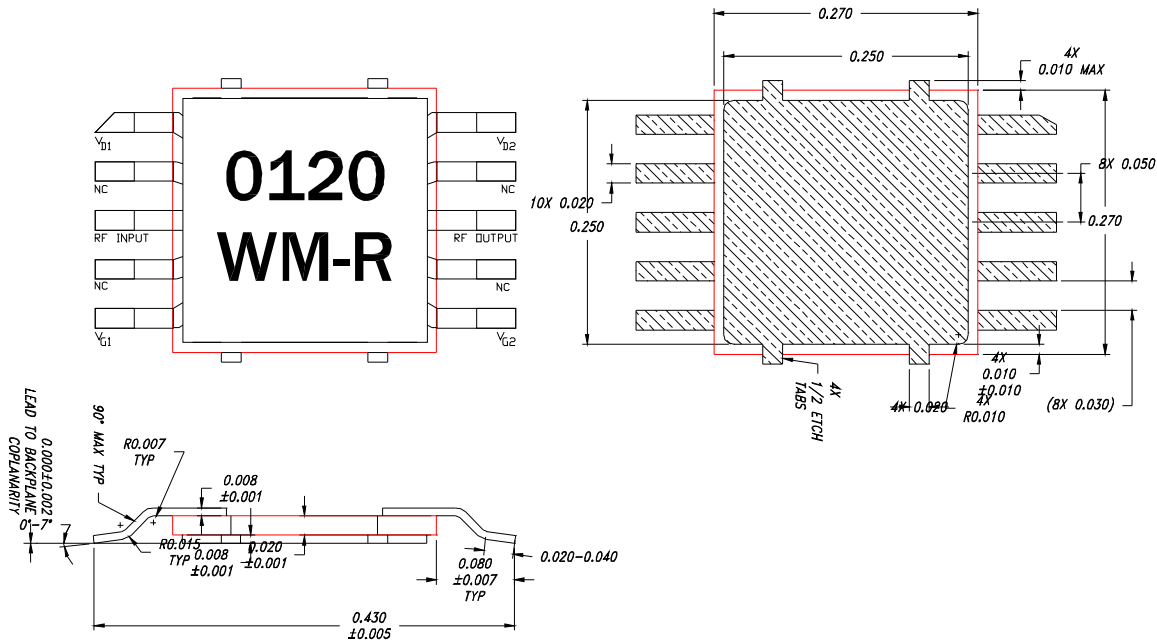


Figure5: Output IP3 vs. Frequency at different drain voltages

PACKAGE OUTLINE



| Pin No. | Function | Bias* |
|---------|----------|--------|
| 1 | Vd1 | +8V |
| 2 | NC | |
| 3 | RF in | |
| 4 | NC | |
| 5 | Vg1 | -1.3V |
| 6 | Vg2 | -1.15V |
| 7 | NC | |
| 8 | RF out | |
| 9 | NC | |
| 10 | Vd2 | +8V |

* V_{g1} & V_{g2} gate biases are for reference only and may vary from lot to lot