Outline

• Introduction

• Two-Step Design Concept:
  - Step-1: 50-ohm unit-cell PA design
  - Step-2: Power combiner / impedance transformer design

• Measured results

• Conclusion
Introduction

- Broadband PA ($f_2 / f_1 \geq 100$) design is a major challenge
- Common approach is Traveling Wave Amplifier (TWA)
- This paper presents an alternative approach, which uses smaller semiconductor real estate, smaller PA size, and lower cost.
- This PA has several potential applications for broadband communications, Software radio, Broadband jammer, Instrumentations ... etc
Basic Design Concept

• The design concept uses a 2-step approach:
• Step-1: Design a unit-cell PA with optimal output 50Ω impedance, such that no matching is required. We use HIFET technique to maximize the output power.
• Step-2: Use broadband push-pull power combiner/impedance transformer to power combine the unit-cell PA, in low impedance environment, to achieve high power.
Output power of unit-cell FET

- Assuming a DC-to-RF power efficiency of 50% we have:
  \[ P_{\text{rf}} = 0.5 \ V_{\text{dc}} \times I_{\text{dc}} \]  
  \[ \text{.......... (1)} \]

- The optimal RF output impedance is proportional to:
  \[ R_{\text{opt}} = \frac{V_{\text{dc}}}{I_{\text{dc}}} \]  
  \[ \text{.......... (2)} \]

- Substituting equation (2) into equation (1), we have:
  \[ P_{\text{rf}} = \frac{V_{\text{dc}}^2}{2 \ R_{\text{opt}}} \]  
  \[ \text{.......... (3)} \]

- Therefore, the device output power capability is proportional to the square of DC bias voltage and inversely proportional to the circuit impedance.
Step 1: Use HIFET to increase Vd and Tailor Zopt to be 50-ohm

- HIFET is an innovative power combining technique, connecting unit-cell FETs RF & DC in series, yet thermally in parallel.
- DC bias voltage and Zopt are proportional to the number of unit cells. Output impedance could be tailored to be 50Ω. Hence no output matching.
- HIFET enjoys a bonus gain of $10 \log_{10}(N)$ dB.
- HIFET concept applies to all devices such as MESFET, CMOS, LDMOS, GaN, SiC …etc.
HIFET Voltage Waveforms*

\[ V_{out} = 4V_m \]

\[ 3V_m \]

\[ 2V_m \]

\[ V_m \]

\[ V_{in} \]

I-V of a 3mm x 4 MESFET HIFET

Doesn’t it look like a GaN HEMT?
MMIC Schematic
HIFET MMIC PA Design

- 1\textsuperscript{st} stage: 4 x 2mm; 2\textsuperscript{nd} stage: 2 x (4 x 2mm)
- Feedback resistors for: gain flatness, good input & output VSWR and stability
- Input series resistor and inter-stage series resistors for good gain flatness and stability
- Bias provided thru external chokes
- Large blocking capacitors for maximum bandwidth
- \[ P_{\text{out}} = \left( N \cdot V_{\text{ds}} \right)^2 / 2 \cdot Z_{\text{out}} \]
- Stability & device thermal considerations
Output Matching Circuit

- \( Z_{\text{opt}} = N \left( V_{\text{ds}} - V_{\text{knee}} \right) / I_{\text{ds}} \)
- We have 2 degrees of freedom: \( N \) & \( I_{\text{ds}} \) (Device size)
- In this 2-stage MMIC PA: output stage is 2 x (4 x 2mm). Hence \( V_{\text{ds}} = 5V \), \( I_{\text{ds}} = 0.36A \), \( V_{\text{knee}} = 0.5V \)
- \( Z_{\text{opt}} = 4 \left( 5 - 0.5 \right) / 0.36 = 50 \ \Omega \)
- No output matching is needed because the device output impedance is designed to be 50\(\Omega\)
- Very small chip size: 2.30 x 2.27 mm
MMIC Process (WIN, PHEMT)

- 0.5µm gate length (Ti-W), double-recess
- Epitaxial and thin film Nichrome resistors
- Silicon Nitride capacitor and passivation
- $I_{dss} \sim 200 – 250mA/mm$
- 4 mils substrate
- Via hole for source ground
Packaged MMIC & Test Fixture

Package size
7 x 7 mm

10mils FR4 substrate
Power and Efficiency vs Freq. (20V/650mA)

- **P3dB (dBm)**
- **Efficiency (%)**
- **Frequency (GHz)**

- **P1dB**
- **Efficiency @ 3dB**
- **Efficiency @ 1dB**
Step 2 – Broadband Power combiner / Impedance transformer
8-Way Combiner/Divider

\[ P \alpha N^2 \]
2-Way Combiner/Impedance transformer (Back to Back)
Performance of 2 Broadband Baluns
Back-to-Back

S21
S11
S22

Frequency (MHz)
Return Loss (dB)
Loss (dB)
Schematic of 10W BB PA
Small Signal Gain, Return Loss vs Frequency (24V/2.9A)
Conclusion

• We presented the approach to achieving ultra-broadband. High-power PA, as well as the measured state-of-the-art results.

• The basic approach is to develop a HIFET 50-ohm device (Unit-cell PA), then use push-pull combiner / impedance transformer to power combine the unit-cell PA’s.

• The unit-cell MMIC PA has 3W P1dB from 20 to 3500MHz with 24dB gain and good linearity

• The power combined PA module has 10W P1dB from 20 to 3500MHz with 23dB gain and good linearity

• This design concept can be applied to GaN HEMT for very high power, and to CMOS to overcome low-voltage operation
Low Frequency Small Signal

Gain & Return Losses (dB)

Frequency (GHz)

Gain

Input RL

Output RL