Three Dimensional Transmission Lines and Power Divider Circuits

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Abstract — We report the development of a number of novel broadband 3D circuits. We present the performance of a 3D X-band 4-way Wilkinson Divider. Excellent performance is also obtained from a delay line, and broadband coupled lines. We also introduce, for embedded transmission lines, a measurement of line losses, and an improved model for analysis and synthesis.

I. INTRODUCTION

The recent boom in wireless communications underscores the need for providing inexpensive microwave circuits and higher levels of on-chip integration. A promising approach is to build three dimensional microwave circuits by laminating multiple microwave circuit layers on top of each other while keeping all active devices on the semiconductor layer.

The 3D approach lowers cost by saving valuable real estate space [1]. This area is receiving increased theoretical attention [2]-[3]. Several multilevel MMIC circuits have been reported [4]-[6]. We have developed [3] a model for the effective dielectric constant and characteristic impedance. In this paper we present an improved model that is twice as accurate as that in [3]. In addition, we develop a method for synthesizing ETL lines to a desired effective dielectric constant. We also measure loss. Finally, we use the unique aspects of the 3D environment to realize some special elements including a broadband vertical balun circuit, a three-layer 4-way Wilkinson divider, a long delay line, a compact pair of coupled lines.

II. ANALYSIS AND SYNTHESIS OF 3D LINES

Three dimensional transmission lines are most easily realized by laminating multiple dielectric layers on top of each other while keeping all active devices on the semiconductor layer (see Figure 1). RF Lines on the first layer are in the embedded transmission line (ETL)

configuration while the upper layers are in a simple stripline configuration. We have developed earlier [3] a model for the effective dielectric constant and characteristic impedance. Here we present an improved model that is twice as accurate as that in [3]. In addition, we develop a method for synthesizing ETL lines to a desired effective dielectric constant.

The closed form empirical expressions we derived earlier [3] are based on the variational method. We obtained the following expression for ε_{eff}

$$\varepsilon_{eff} = \left(\frac{\varepsilon_1 + \varepsilon_2}{2}\right) \cdot \frac{U(K(\varepsilon_1, \varepsilon_2))}{U(K(1,1))} \tag{1}$$

$$U(x) = 1.15 - \ln(x) + 0.08 \cdot x^2 \tag{2}$$

$$K(\varepsilon_1, \varepsilon_2) = \frac{1}{\varepsilon_1 + \varepsilon_2} \cdot \left[\frac{\varepsilon_1}{\left(\frac{2h}{w}\right)} + \frac{\varepsilon_2}{\left(\frac{2d}{w}\right)}\right] \tag{3}$$

where h, d, w, ε_1, ε_2, are the GaAs thickness, polyimide thickness, line width, GaAs dielectric constant and polyimide dielectric constant, respectively. Comparing the values obtained from the previous expression for ε_{eff} with those calculated by full wave EM simulation using Sonnet^{TM}, for a wide variety of practical line widths and polyimide thicknesses, we observed an error less than 1% for $K(\varepsilon_1, \varepsilon_2) < 1$ (in typical cases, this will include the range of $0.1 < w/h < 2$ and $0.1 < w/d < 2$). The form and coefficients of $U(x)$ were derived based on the series expansion of the variational method expression. By allowing ourselves to include more terms and optimise coefficients (instead of simply truncating the series) of $U(x)$ against a very large number of empirical results, we find that a more accurate expression can be derived,

$$U(x) = 1.15 - 1.074\ln(x) + 0.13 \cdot x^2 - 9.25 \cdot 10^{-3} \cdot x^4$$
(4)

The new definition of $U(x)$ reduces the maximum observed error to 0.5% (instead of 1%) in all cases (the same restriction that $K(\varepsilon_1, \varepsilon_2) < 1$ still applies). Thus we have reduced the error by 50% with a simple modification to Equation (2).

Next, we develop a method for synthesizing ETL lines to a desired effective dielectric constant by 'inverting' Equation (1). After some lengthy manipulation, we develop the following synthesis equations for ETL line width w,

$$w = \frac{4hd}{d+h} \cdot \exp(F - G)$$
(5)

where,

$$F = \xi\left[2Q\left(\varepsilon_{eff} R^2 - \varepsilon_{avg}\right)\exp(G)/25 \right]$$
(6)

$$\xi(x) = y \text{ such that } \left(y \cdot e^y - x = 0\right)$$
(7)

$$R = \frac{\varepsilon_1 d + \varepsilon_2 h}{\varepsilon_{avg}(d+h)}$$
(8)

$$G = Q\varepsilon_{eff}\ln(R) + 2.3$$
(9)

$$Q = 2/(\varepsilon_{avg} - \varepsilon_{eff})$$
(10)

$$\varepsilon_{avg} = (\varepsilon_1 + \varepsilon_2)/2$$
(11)

The above set of equations is the exact inverse of equations (1)-(3) and hence there is no deterioration in accuracy.

III. 4-WAY WILKINSON DIVIDER DESIGN AND EXPERIMENT

We designed a 3D 4-way Wilkinson divider using an Alumina-Ployimide thin film process. One of the challenges of planar circuits, which is easily overcome in 3D circuits, is designing 1-to-N way combiners where the line length of each arm is kept constant. In a Wilkinson divider, all the arms are the same length and are connected together at the input and at the output (to the balancing resistors that provide isolation). The 3D environment facilitates the realization of *equal-length* arms that are connected at input and output. The schematic of a general N-way Wilkinson divider are shown in Fig. 4a. In our case, N=4. We implemented two of the arms of the Wilkinson divider on a 10-mil Alumina substrate, then added 30 microns of Polyimide (ε_r = 3.2), and implemented the other two arms. The line width was selected such that each line has 100-ohm characteristic impedance and quarter wave length at 10.75 GHz. Via holes were used to connect the lines and to connect to the resistors. EM simulation was carried out using Sonnet and Ansoft's HFSS. The layout, picture and measured performance are shown in Figs. 4b, 4c, and 4d.

The overall size of the Wilkinson divider circuit is 0.1" x 0.1". This is similar to the size of conventional 2-way Wilkinson divider built using planar circuit topology. A 4-way Wilkinson, built using planar topology would be difficult to build and larger in size. The 3D technology, in general, offers higher integration advantages.

IV. DELAY LINES, COUPLERS, AND LINE LOSS

Three-dimensional MMICs and hybrids are inherently compact in size due to several reasons. First, moving matching circuit elements to upper layers reduces the circuit's footprint. Second, reducing a layer's thickness, h, reduces the width, w, of transmission lines since the characteristic impedance is a function of w/h. Last, the minimum spacing, typically $2h$, needed between lines to prevent undesirable coupling is directly proportional to h. All of these factors combine to produce a much smaller chip footprint. This chip miniaturization may introduce some undesirable effects; mainly an increase in ohmic losses. To assess that, we fabricated a 50-ohm 1mm-long delay line in the ETL configuration where there is one layer of polyimide covered with ground (Figure 1) with ε_{GaAs} = 12.9, $\varepsilon_{Poly.}$ = 3.2, w = 7μm, d = 6μm, and h = 100μm. The loss was -0.2 dB/mm at 5 GHz, -0.32 dB at 10 GHz, and -0.4 dB at 15 GHz. Compared to a 50-ohm line on GaAs MMIC, w = 73μm, the loss is higher by a factor of about four. Despite the reduction in line width by a factor of ten, the loss increases by a factor of four only. Due to the small substrate thickness 3D circuits may be more suitable for circuits with low Z_o lines. In fact, 3D technology enables the designer to realize lines with Z_o as low as a few ohms. This is in sharp contrast to microstrip lines on a 100μm GaAs MMIC where the minimum practical Z_o on is about 25 ohms.

A good demonstration of the compactness of 3D technology is to build a long delay line. Figure 5 shows the performance of a 19mm long 50-ohm line occupying only 0.5 mm^2. Despite the loss, one is able to accumulate significant phase delay. For example, at 2.75 GHz we have 90°-phase shift and -1.5 dB series attenuation (or -0.75 dB attenuation if used for biasing as a shorted quarter wave stub).

Realizing strong coupling is another area of strength for 3D technology. This is demonstrated with a pair of coupled lines. Figure 6a, and 6b show the layout and performance of a 1.7mm long pair of coupled lines occupying only 0.2 mm^2. The coupled lines split the power evenly between the *coupled-* and *through*-port over

a very wide bandwidth (10 to 30 GHz).

V. CONCLUSION

We presented an improved model for modeling 3D embedded transmission lines as well as synthesis equations. We also developed a broadband 3D balun that relies on a novel concept of vertical coupled transmission lines. The measured results confirm the usefulness of the concept and points to the need to reduce any radiation-based loss. We also designed and tested a 3D X-band, multi-layer, 4-way, Wilkinson divider. The 3D concept can be easily expanded to N-way division, where N=5, 6, 7, etc. In addition, we presented a very compact delay line and coupled lines. In general, the 3D/multilayer topology offers much greater flexibility than the conventional planar topology. This particularly true in passive components (e.g. filters, couplers, dividers, etc.). Currently, the lack of theoretical models is an obstacle to the development of more advanced 3D microwave circuits.

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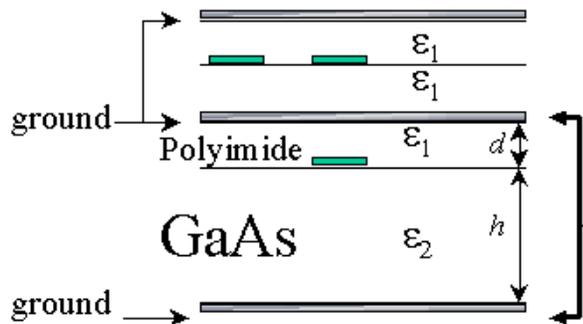
Fig. 1. Schematic of a three-dimensional circuit.
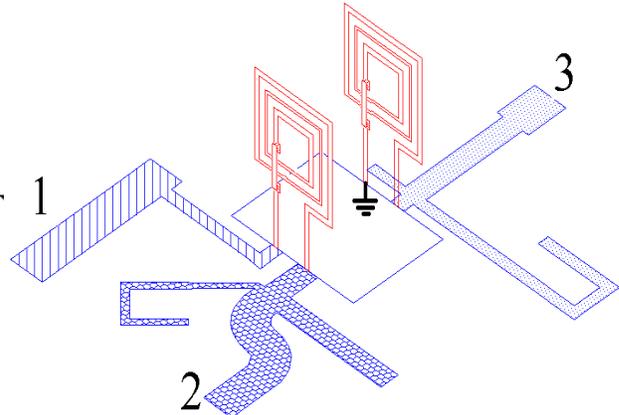

Fig. 2c: Vertical balun concept: layout of vertical balun design.
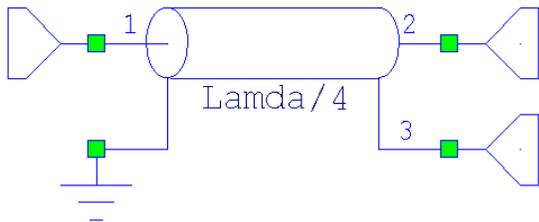

Fig. 2a: Conventional balun design configuration.
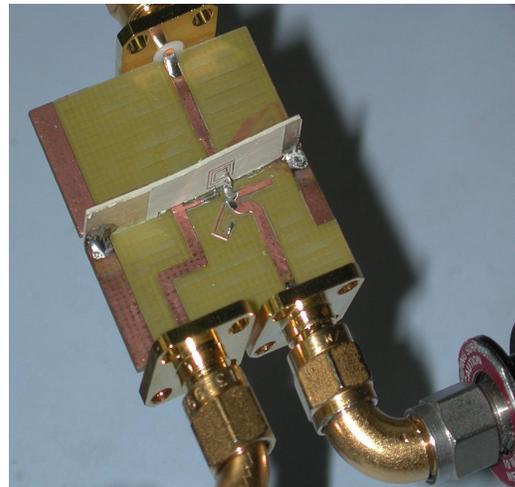

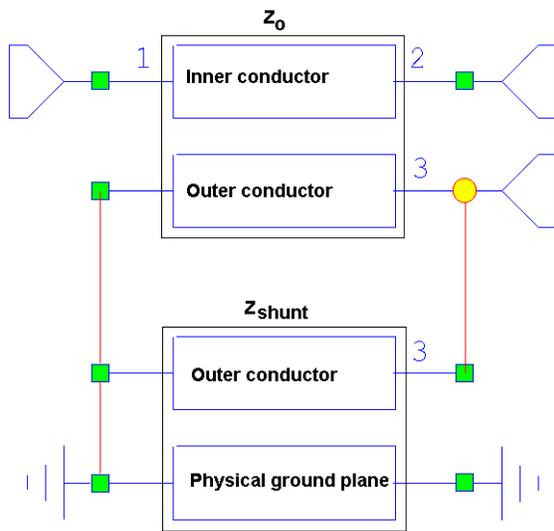Fig. 2d: Vertical balun concept: picture of finished balun.

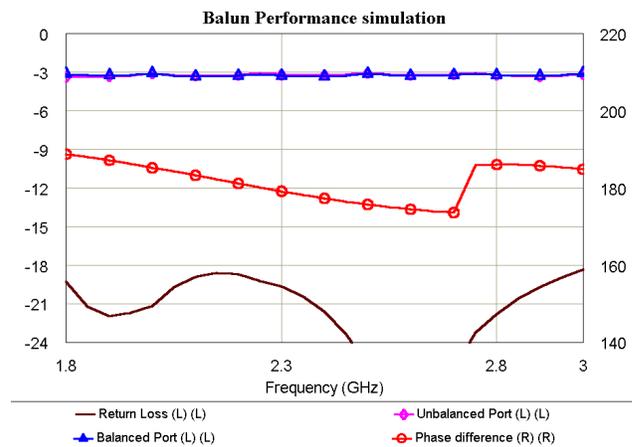
Fig. 2b: Conventional balun equivalent circuit.

Fig. 3a: Simulated vertical balun performance. The return loss is better than –15 dB, and phase variation is –/+ 7 degrees over 1.8 GHz to 3 GHz bandwidth.
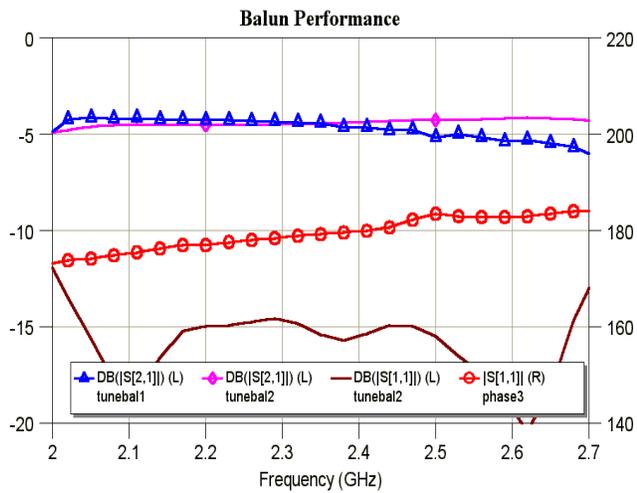
Fig. 3b: Measured vertical balun performance. The return loss is –15 dB, and phase variation is –/+ 5 degrees.
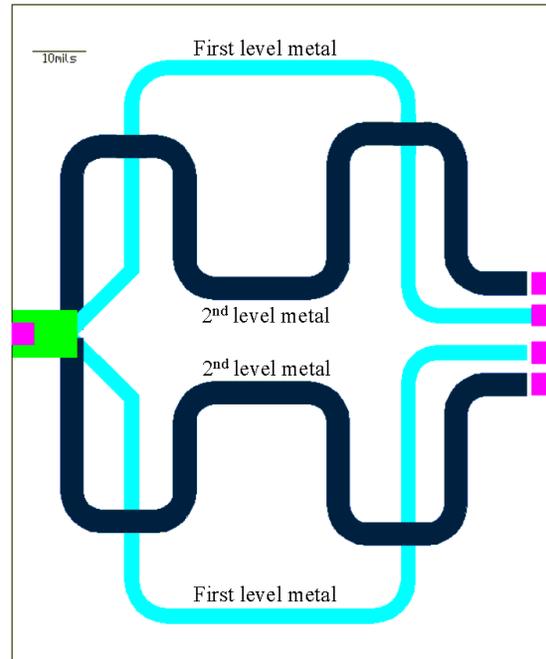
Fig. 4b. 3-layer X-band 4-way Wilkinson divider layout (the isolation resistors are hidden). Each line has a characteristic impedance of 100-ohm.
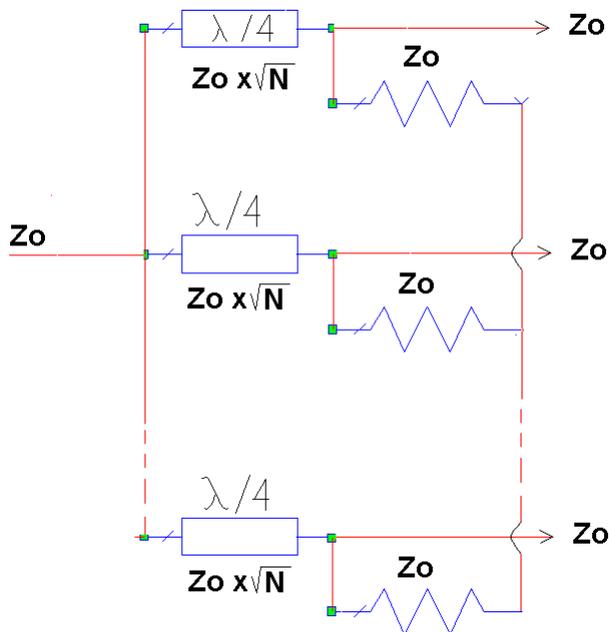
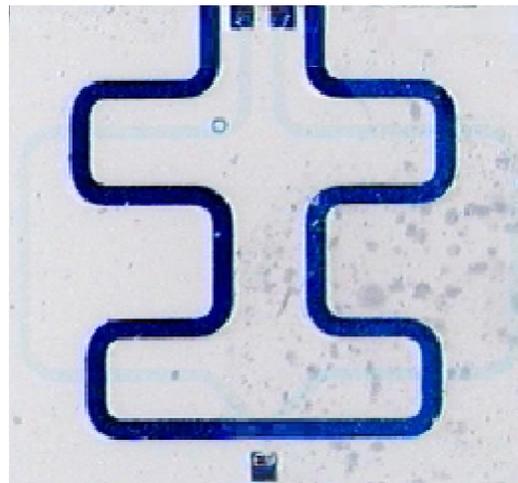Fig. 4a. General N-way Wilkinson divider schematic. In our case, N=4.

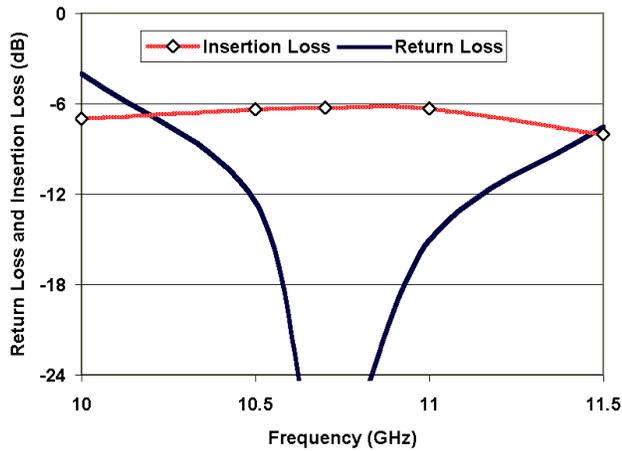Fig. 4c. Picture of finished 3-layer X-band 4-way Wilkinson divider. Off chip resistors used are not shown.

Fig. 4d. 3-layer X-band 4-way Wilkinson divider measured performance (for all arms of the Wilkinson, the insertion loss is about 6 dB, as expected from a 4-way divider, and return loss is about –15 dB).
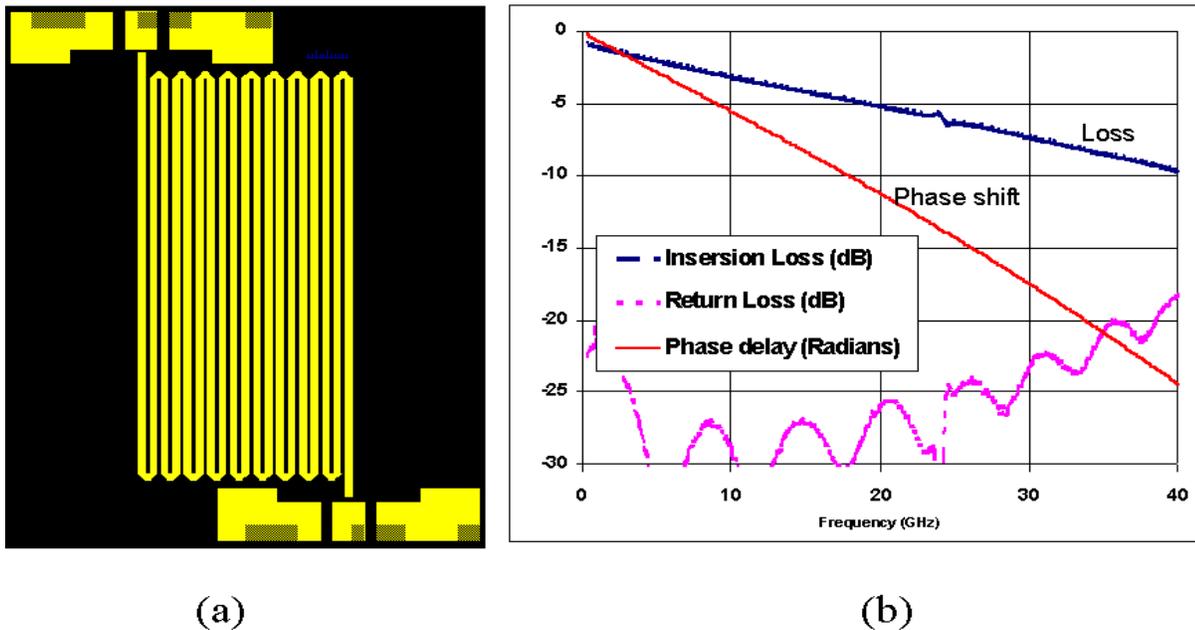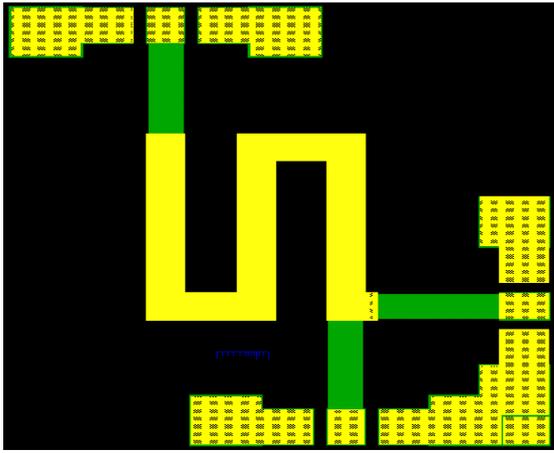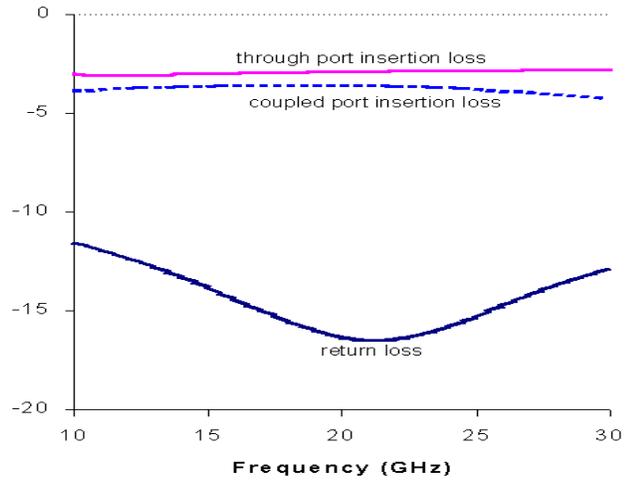

(a)   (b)

Fig. 5. A compact delay line, 19mm long, performance. Measured input return loss (dB), insertion loss (dB), and phase shift (radians).

Fig. 6. Coupled lines (a) layout, (b) and measured performance.