UHiFET – A New High-Frequency High-Voltage Device

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***Abstract* — The HiFET (High-Impedance, High-Voltage FET) configuration is used to connect several semiconductor FETs both DC and RF in series, resulting in high DC bias voltage and high output impedance. The HiFET power and efficiency degrades at high microwave frequencies (i.e. > 3GHz) due to gate leakage currents. In this article, we propose a new configuration, the Universal HiFET (UHiFET), which uses an additional compensation to equalize the RF voltages and currents of all the transistor cells that are connected in series. This new approach improves the power, efficiency and linearity of the original HiFET configuration at microwave and millimeter wave frequencies. We are presenting a mathematical analysis of the UHiFET and measured data to demonstrate the effectiveness of the proposed approach.**

***Index Terms* — Broadband amplifiers, high-voltage techniques, microwave devices, power combiners, MMICs.**

I. Introduction

Several techniques have been used to stack several devices in series to raise the operating voltage [1-3]. The HIFET [3] technique connects several GaAs or CMOS FETs both DC and RF in series to achieve high impedance and high DC bias voltage (Fig. 1).

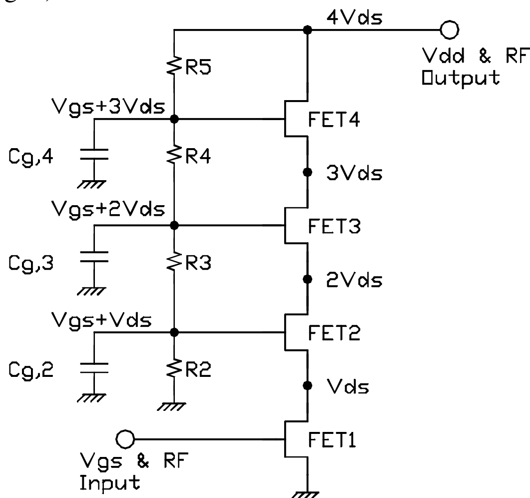

Fig. 1. Original High-voltage device (HiFET) concept

This technique raises the operating voltage while efficiently combines the power of individual devices to achieve high power levels not possible with conventional devices.

The HiFET works perfectly at low frequencies (i.e.< 3GHz) and the concept was applied successfully using GaAs and CMOS MMICs as outlined in references [4 - 7]. However, the configuration suffers from decreased power levels and efficiency at higher frequencies. Sections II gives a brief description of a new HiFET configuration which exhibits excellent performance at microwave frequencies, Section III gives a theoretical analysis of the new concept, and Section IV shows the implementation of two devices in-series and presents the measured power and efficiency of the new configuration at 7GHz. This new concept is applicable to any bipolar or field effect transistor technology.

II. UHiFET Configuration

Fig. 2 shows the UHiFET with new compensation circuit.

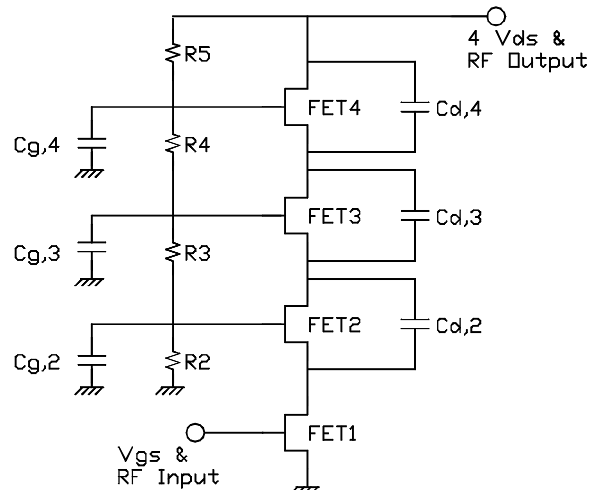

Fig. 2. Universal high voltage FET (UHiFET)

In order to properly combine the output power of all the series device cells, the RF voltage and current of all devices must be same magnitude and in-phase. At higher frequencies, the RF voltage and current of each unit cell become slightly out-of-phase relative to its adjacent cell leading to inefficient power combination of the cells. This out-of-sync voltage and current waveforms are caused by the gate leakage in the successive series devices due to $C_{g,2}$, $C_{g,3}$ & $C_{g,4}$ capacitors in Fig. 1. This leakage is negligible at low frequencies this is where the HiFET works fine. To offset the gate current leakage, we propose to add C_{d2}, C_{d3} & C_{d4} as shown in Fig. 2 to equalize the devices at microwave and millimeter wave frequencies. We call this high-frequency HIFET the Universal HIFET: "UHIFET". The compensation works by designing

$C_{d,2}$ to conduct a current equal to the gate current of FET2 , and $C_{d,3}$, $C_{d,4}$ to equalize the gate currents of FET3 and FET4 respectively.

III. THEORETICAL CONSIDERATION

Let us analyze a generalized UHiFET configuration consisting of several devices in series as shown in Fig. 3.

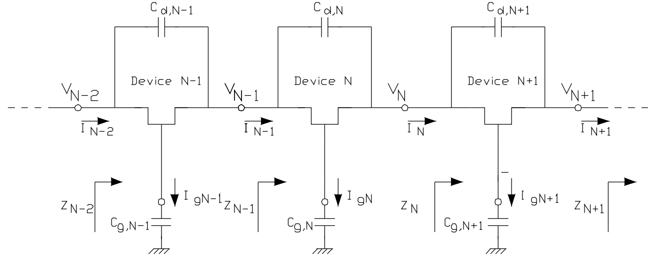

Fig. 3. Several-Cell UHiFET Schematic

Fig. 4 shows the RF equivalent circuit of a typical FET and Fig. 5 shows the equivalent circuit of the UHiFET in Fig. 3.

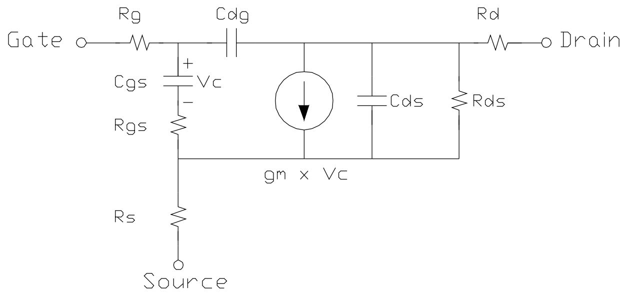

Fig. 4. Intrinsic Small-Signal FET Equivalent Circuit

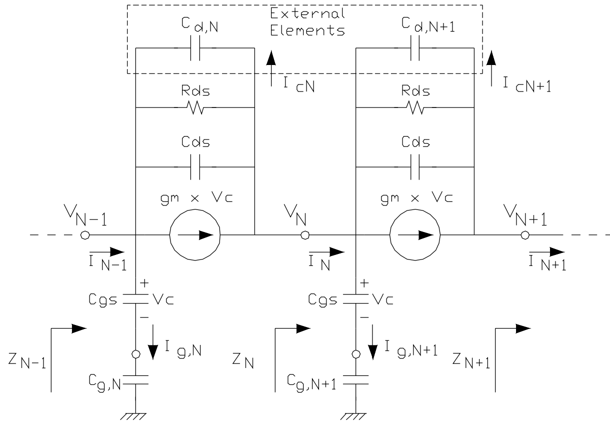

Fig. 5. Small-Signal Equivalent Circuit of an N-Cell UHiFET

For the sake of simplicity R_g, R_d , R_s, R_{gs} & C_{dg} is ignored in Fig. 5 since they have a small effect on device performance and can safely be ignored in the following analysis. The effects of these parasitic elements could easily be included in computer simulations; they are ignored in our analysis to illustrate how the new technique works.

To achieve maximum power out of an M-Cell UHiFET the voltage swings across device terminals, the current source g_m V_c , and the currents flowing through the intrinsic elements in each device should be identical for all devices. However, the currents flowing through the $C_{d,N}$ compensating elements need not be the same. Actually the currents flowing through these $C_{d,N}$ elements are critical in restoring the device synchronism and voltage balance at microwave frequencies. Based on the above the following conditions should apply:

$$V_{N+1} - V_N = V_N - V_{N-1} = V_m \tag{1}$$

V_m is the voltage swing across drain and source of each device. Hence

$$V_N = N \cdot V_m \tag{2}$$

For equal device currents V_c is a constant:

$$V_c = V_{gs,N} = \frac{(N-1)V_m}{1 + \frac{C_{gs}}{C_{g,N}}} \tag{3}$$

Since V_c is constant the current sources in all cells have the same magnitude I_m

$$I_m = g_m V_c = g_m \frac{(N-1)V_m}{1 + \frac{C_{gs}}{C_{g,N}}} \tag{4}$$

Assume that Y_{opt} is the optimum impedance needed at the drain terminal of a common source single FET (i.e. FET No. 1 in the UHiFET configuration) hence by definition:

$$Y_{opt} = (I_m - j\omega C_{ds} V_m) / V_m \tag{5}$$

From (4) & (5)

$$Y_{opt} + j\omega C_{ds} = g_m \frac{(N-1)}{1 + \frac{C_{gs}}{C_{g,N}}} \tag{6}$$

Hence

$$C_{g,N} = \frac{C_{gs}}{g_m (N-1)/(Y_{opt} + j\omega C_{ds}) - 1} \tag{7}$$

Notice that for all microwave transistors Y_{opt} can be approximated by a shunt resistor and a shunt negative capacitor defined as follows:

$$Y_{opt} = G_{opt} - j\omega C_{opt} \tag{8}$$

Usually $C_{opt} \approx C_{ds}$ so from (7) & (8)

$$C_{g,N} = \frac{C_{gs}}{g_m (N-1)/(G_{opt} - j\omega C_{opt} + j\omega C_{ds}) - 1} \cong \frac{C_{gs}}{g_m (N-1)/G_{opt} - 1} \quad (9)$$

Referring to Fig. 5 from Kirchhoff's current law the current I_N coming from the Nth cell is:

$$I_N = g_m V_c - (j\omega C_{d,N} + j\omega C_{ds}) V_m \quad (10)$$

That same current should be sinking into the $(N+1)^{th}$ cell that is:

$$I_N = g_m V_c + j\omega C_{gs} V_c - (j\omega C_{d,N+1} + j\omega C_{ds}) V_m \quad (11)$$

From (10) & (11)

$$j\omega C_{d,N+1} V_m = j\omega C_{d,N} V_m + j\omega C_{gs} V_c \quad (12)$$

Equ. (12) simply states that for perfect synchronization the current of the $C_{d,N+1}$ compensating capacitor is needed to feed the compensating capacitor of the Nth cell (i.e. $C_{d,N}$) and the gate current of the $(N+1)^{th}$ cell. From (12) & (3):

$$j\omega C_{d,N+1} = j\omega C_{d,N} + j\omega C_{gs} \frac{(N-1)}{1 + \frac{C_{gs}}{C_{g,N}}} \quad (13)$$

From (13) & (6)

$$j\omega C_{d,N+1} \cong j\omega C_{d,N} + j\omega C_{gs} G_{opt} / g_m \quad (14)$$

Since $C_{d,1} = 0$

$$j\omega C_{d,N+1} \cong \frac{j\omega C_{gs}}{g_m} N G_{opt} \quad (15)$$

From (2) & (11) we could calculate the admittance presented at the drain of every cell Y_N:

$$\begin{aligned} Y_N &= 1/Z_N \\ &\cong (G_{opt} - j\omega C_{ds})/N - j\omega C_{d,N}/N \quad (16) \\ &\cong Y_{opt}/N - j\omega C_{d,N}/N \end{aligned}$$

From (16) we deduct that the optimum impedance for the Nth-Cell UHiFET is N times the optimum impedance of a single device in parallel with a negative capacitance equal to $C_{d,N}/N$.

The above analysis of the UHiFET shows how to improve the HiFET to obtain good power and efficiency at any frequency in the microwave and millimeter wave spectrum.

IV. Experimental Verification

To verify the validity of the proposed UHIFET concept, we designed test patterns using 0.5µm gate GaAs pHEMT. These test patterns include a 3mm gate-width PHEMT as control , a two-in-series (3mm each) HiFET without compensation, and a two-in-series UHIFET with compensation. Figs. (6 - 8) show the layouts of the 3 test cells.

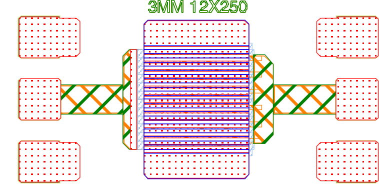

Fig. 6. Layout of a single 3mm FET

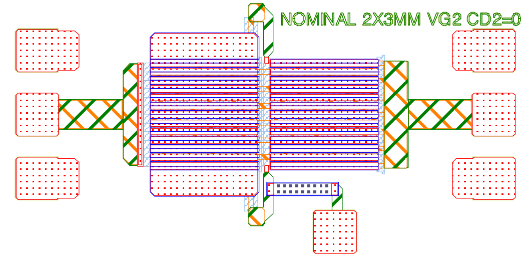

Fig. 7. Layout of a 2x3mm HiFET

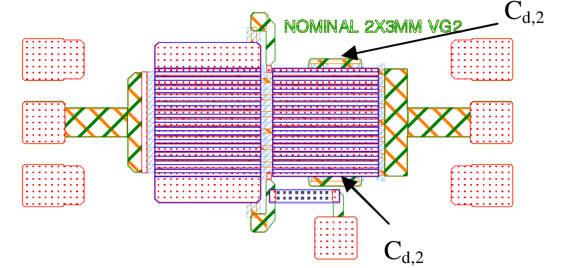

Fig. 8. Layout of a 2x3mm UHiFET

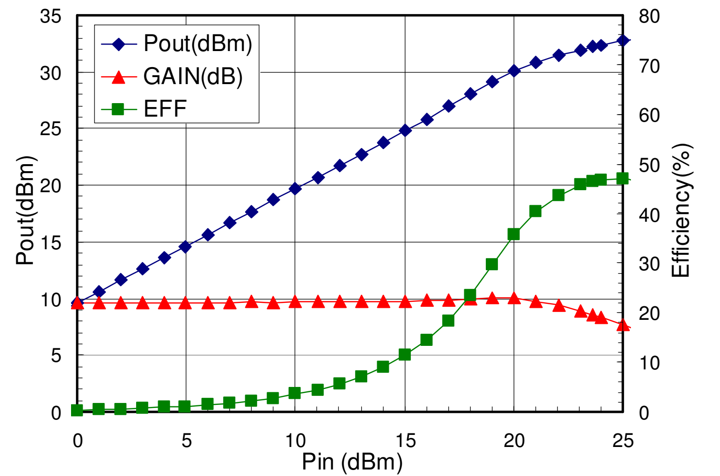

Fig. 9. Performance of a single 3mm pHEMT @7GHz (V_{dd}=+8V, V_{gs}=-0.95V, I_d=0.4A)

Fig. 9 shows the performance of the 3mm pHEMT at 7GHz. We used the load-pull system to achieve the best performance for each test pattern. This 3mm PHEMT serves as the baseline information. The small signal gain is 9.5dB, P_{1dB}=32dBm, efficiency at P_{1dB} =50%.

Fig. 10 shows the performance of the un-compensated 2x3mm HiFET. The small signal gain is 14dB, P_{1dB}=34dBm, efficiency=44%. Notice that the output power P_{1dB} of 34dBm is not twice that of the single 3mm device (32dBm). The efficiency of 44% is also degraded from the 3mm device (50%). This indicates that the performance of the un-compensated 2-in-series HIFET is degraded at 7GHz.

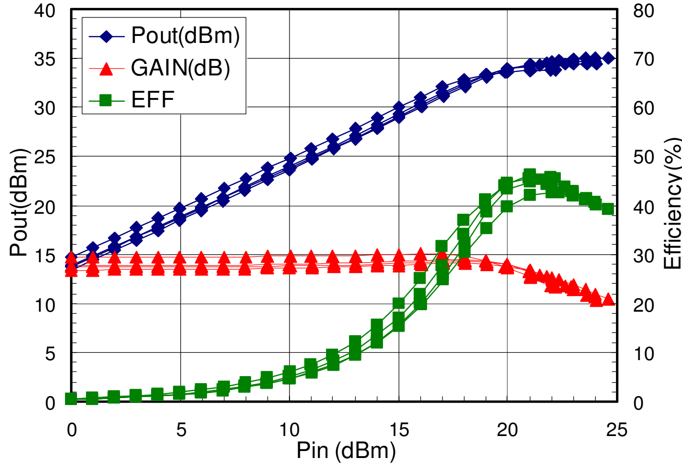

Fig. 10. Performance of uncompensated 2x3mm HiFET @7GHz (V_{dd}=+16V, V_{gs}=-0.95V, I_d=0.4A)

Fig. 11 shows the performance of the compensated 2x3mm UHiFET. The small signal gain is 14dB, P_{1dB}=35dBm, efficiency=60%. This clearly shows that the UHiFET performance at 7GHz is better than the un-compensated HiFET. The above performance is summarized in Table 1 for clarity. Notice also that HiFET & UHiFET have higher gains than the single device as explained in [3].

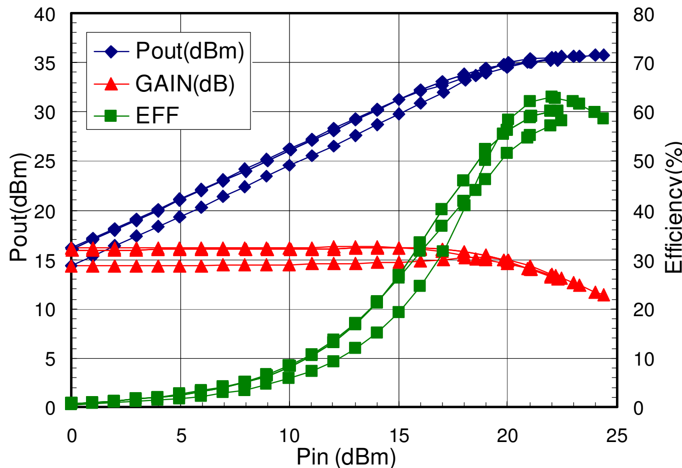

Fig. 11. Performance of compensated 2x3mm UHiFET @7GHz (V_{dd}=+16V, V_{gs}=-0.95V, I_d=0.4A)

Table 1. Summary of Performance

Configuration	3mm FET	2x3mm HiFET	2x3mm UHiFET
Gain	9.5dB	14dB	14dB
P1dB	32dBm	34dBm	35dBm
Efficiency@P_{1dB}	50%	44%	60%
V_{dd}	+8V	+16V	+16V
I_{dd}	0.4A	0.4A	0.4A

IV. Conclusion

We demonstrated a new configuration to improve the performance of the HiFET at any frequency by including a simple compensation circuit. Excellent power and efficiency were demonstrated at 7GHz for a 2x3mm UHiFET.

Acknowledgement

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