Advances in Microwave & Millimeter-wave Integrated Circuits

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***Abstract* — This tutorial paper reports on the state-of-the-art of Monolithic Microwave Integrated Circuits (MMIC) technology. The paper gives an overview of available MMIC semiconductor materials, devices, processes and outlines the steps of a typical MMIC manufacturing process followed by a description of the different technologies used in MMIC assembly and packaging. MMIC design guidelines regarding performance and cost are also presented. A recent literature survey of MMICs used for wireless, microwave and millimeter-wave applications is shown to emphasize the merits of different MMIC technologies. Several examples of novel devices and design techniques are presented and the paper concludes with future trends in this field.**

***Index Terms* — MMIC, MMIC Design, MMIC LNA, MMIC power amplifiers, Monolithic Microwave Integrated Circuits.**

I. Introduction

The impact of the integrated circuit could be felt in all aspects of modern life from entertainment media, consumer electronics and wireless equipment to aerospace communications and cutting edge scientific applications. Monolithic Microwave Integrated Circuits (MMIC) are a special type of analog ICs that process signal frequencies from below 1GHz to 300GHz [1]. The first MMICs were reported in 1968 [2] & [3] and the first transistor based MMIC was demonstrated in 1976 [4]. During the early 1980s MMICs were used mainly for satellite and military applications, but in the early 1990s with the development of mobile and wireless communications, GaAs MMICs were mass-produced for the first time. Due to their relatively small size MMIC contributed to the miniaturization of RF and microwave circuits. MMICs can perform all analog functions required by a typical communications system such as: mixers, gain blocks, power amplifiers, low noise amplifiers, attenuators, phase shifters, switches, VCOs, up-converters, down-converters. Single MMICs are cheap in large scale production and are most useful for applications where small size, large quantity and medium power levels are needed (i.e. < 10W). Power applications of the order of 100W to 1000W are still the domain of hybrid circuits using discrete devices and conventional MIC technology. High power applications (i.e. >1kW) are dominated by vacuum tubes such as the TWT and the magnetron.

Section II in this paper introduces the different semiconductors and active devices used in MMICs. Section III describes MMIC manufacturing and packaging and gives a brief survey of available MMIC foundries. Section IV outlines important design guidelines that MMIC designers need to consider before applying MMIC technology to a particular application. It also gives a brief description of the design steps that engineers should follow in order to translate a new idea from engineering prototype to successful system insertion and product manufacturing. Section V surveys state-of-the-art MMICs as reported in the literature and shows samples of novel MMICs for different applications and section VI offers some insight into future trends and a conclusion.

II. MMIC Semiconductors and Devices

MMICs are manufactured on semiconductor materials to integrate active devices such as bipolar or field effect transistors with passive elements to perform analog functions such as signal amplification, up & down-conversion, switching, attenuation …etc. MMIC substrate materials must behave like a dielectric with reasonable low losses at microwave and mm-wave frequencies. Table 1 shows different semiconductors for MMIC manufacturing and their important physical and electrical characteristics [5-6]. Gallium Arsenide (GaAs) was the first material to be used in MMIC manufacturing 40 years ago due to its superior transport characteristics and its low loss at microwave and mm-wave frequencies. In the last 10 years sub-micron RF CMOS devices and SiGe bipolar devices MMICs are offering a strong competition [7]. Silicon based MMICs, however, are constrained to low power applications due to high RF loss in Silicon substrate. For power applications GaAs technology is still the preferred choice. Bipolar or field effect transistors (FET) are manufactured on most semiconductors with varying degrees of difficulty. Recent advances show the feasibility of Si LDMOS MMICs for applications up to 3GHz [8-11]. Wide band-gap materials such as Silicon Carbide (SiC) and Gallium Nitride (GaN) have applications for high power but these semiconductors are expensive. Silicon Carbide (SiC) is used for high power but is limited to below 5GHz applications [12] and Gallium Nitride (GaN) is promising to push the power limit of MMICs at microwave and mm-wave frequencies. In the last few years many research papers were published on GaN devices and materials and few MMICs have been reported [13 – 15], but low cost GaN MMICs are not available yet due to the high cost of growing pure GaN wafers or depositing GaN layers on SiC substrates, and due to reliability and process issues. GaN deposited on Semi-insulating Silicon wafers could offer low cost MMIC. Other semiconductors such as Indium Phosphide

(InP) [16] and Antimonide base semiconductors (ABSC) on GaAs are in research stage and their applications are limited to 100GHz frequencies or to very low power consumption such as in ABSC [17].

Table 1: Semiconductor Materials for MMIC

MMIC Semiconductors	Electron Mobility	ε_r	RF Loss	Thermal Conductivity	Active Device Technology	Application
Gallium Arsenide (GaAs)	$0.85m^2/V/s$	12.9	Low	46 W/ºC/m	MESFET, HEMT, pHEMT, HBT, mHEMT	PA, LNA, mixers, attenuators, switches, …etc
Silicon (Si)	$0.14m^2/V/s$	11.7	High	145 W/ºC/m	LDMOS, RF CMOS, SiGe HBT (Bi-CMOS)	Mature for low power mixed signal applications
Silicon Carbide (SiC)	$0.05m^2/V/s$	10	Low	430 W/ºC/m	MESFET	Very high power below 5GHz
Indium Phosphide (InP)	$0.60m^2/V/s$	14	Low	68 W/ºC/m	MESFET, HEMT	mm-wave
Gallium Nitride (GaN)	$0.08m^2/V/s$	8.9	Low	130 W/ºC/m	HEMT	High power, limited availability

Active devices used in MMIC applications are mainly FET or bipolar types. FET and Bipolar transistors have different names depending on gate type and device active layer structure. Most Silicon FET devices use Metal-Oxide Semiconductor (MOS) structures. Examples of FET transistor types on Silicon are the RF CMOS (same as used in digital circuits but small gate length) and most recently LDMOS. Most GaAs FETs have Schottky barrier for the gate since no gate insulator could be successfully deposited on GaAs surface. Many GaAs FET types were developed such as the Metal-Semiconductor Field Effect Transistor (MESFET), the High-Electron Mobility Transistor (HEMT), the Pseudomorphic High-Electron Mobility Transistor (pHEMT). Examples of bipolar transistors types are the SiGe Heterojunction Bipolar Transistor (HBT) and the GaAs HBT. GaN and SiC MMICs usually use MESFET or HEMT device structures. Figure 1 shows a common pHEMT structure and Figure 2 shows a typical GaAs HBT structure.

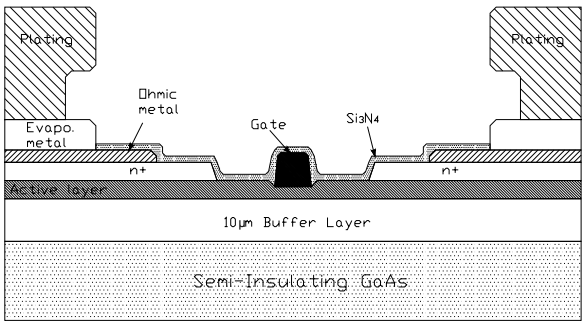


Fig. 1: Typical pHEMT Structure

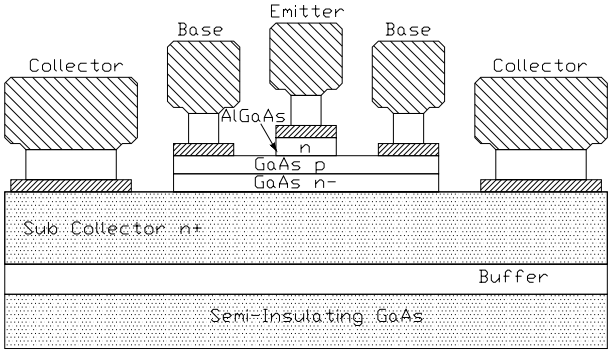


Fig. 2: Typical HBT Structure

Device gate length in FETs or emitter width in BJTs and active region doping dictate the highest frequency a transistor can achieve which are traditionally expressed in terms of maximum frequency of oscillation ($f_{max} \sim g_m (R_{ds} / R_{gs})^{0.5}/4/\pi/C_{gs}$) [18]. For example GaAs FET devices with 1µm gate length give reasonable gain (i.e. > 8dB) only up to X-Band and for higher frequencies sub-micron gates should be used. FET gate length of 0.15µm is needed for 77GHz and 94GHz applications.

III. MMIC MANUFACTURING AND PACKAGING

MMIC manufacturing is expensive, time consuming and could require several iterations to meet the RF specifications, therefore it is critical that the designer selects the proper semiconductor process and the proper active device type. The steps of a typical GaAs MESFET MMIC fabrication process steps are illustrated in Fig. 3. Figure 3a shows the typical material structure for the active region mesa which is usually grown using MBE epitaxy. The active region is defined by etching the surrounding areas or by ion implantation isolation. The fabrication begins with photo resist patterning to define the ohmic contact area, then depositing ohmic contact metal, usually AuGe/Ni/Au by lift-off technique. This defines the FET source and drain contacts. Next, the ohmic contact is sintered to achieve a contact resistance of less than 0.1 ohm-cm (Fig. 3b). Next, the photo resist is patterned to expose the channel region. The N+ layer in the channel region is etched away to expose the active N region (first channel etch). Then the gate region channel is further etched (Fig. 3b), and gate metal is deposited (Ti/Pt/Au or Ti/W/Au) (Fig. 3c). This double recess process controls the current density (Usually 300 mA/mm gate width), as well as provides a reasonable drain-gate break down voltage of about 20 volts. After the gate metallization, a thin (300°A) Si_3N_4 layer is deposited on top of GaAs surface to protect the channel; it is called the passivation layer (Fig. 3c). Next, thin film resistor metal is deposited (Nichrome or Tantalum Nitride) then bottom metal (Ti/Au) (Fig. 3d). A relatively thick Si_3N_4 layer (1500°A-2000°A) is deposited followed by top metallization (Ti/Au). This forms the MIM (Metal-Insulator-Metal)

capacitor. The thick (2-5µm) top metal also serves as the spiral inductor and the matching circuit metallization (Fig. 3e). Finally, the back side of the semi-insulating substrate is thinned from about 12 mils down to 2 – 4 mils (50-100µm) thick (Fig. 3f). Via holes are etched under the FET source region, and Ti/Au are deposited on the back side to connect the source to the back side. The wafer is now ready to be mounted on the blue tape/wafer frame then is ready for dicing. Some foundries add an additional top layer of Polyimide to protect the MMIC surface and in some applications to offer additional layers for 3D applications. MESFET, HEMT, pHEMT active layers are specially designed for LNA, power or switching applications. Table 2 shows the most popular process for a variety of applications.

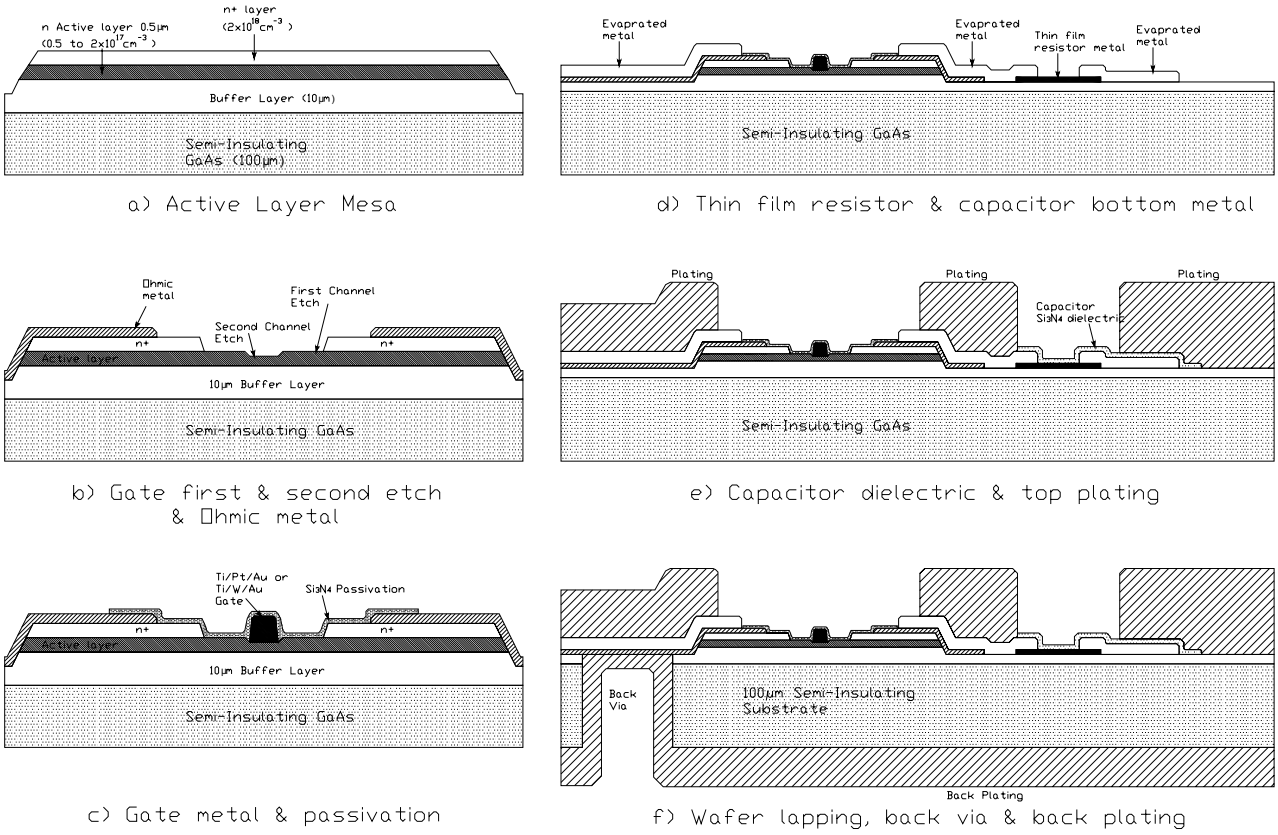


Figure 3: Typical Fabrication Steps for a GaAs MESFET Process

Table 2: Microwave & mm-wave Applications and Recommended Process

Application	Frequency	Device Process
Low Noise Amplifiers	1-10GHz	GaAs Mesfet
	10 –100Ghz	GaAs pHEMT
	> 100GHz	InP
Medium Power	1 -10GHz	GaAs HBT, GaAs Mesfet
	10 – 100GHz	pHEMT
High Power	1 - 10GHz	GaAs Mesfet, GaN, SiC
	10 – 30GHz	GaN
Switches for digital attenuators and phase shifters	0.1 – 20GHz	Mesfet
	20 – 100GHz	pHEMT
Low Power Mixed Signal	1 – 50GHz	SiGe BiCMOS
VCO	1 -100GHz	GaAs HBT

MMIC manufacturing services are offered by many foundries in the USA, Europe and the Far East. Each foundry process is usually defined by the type of active device and device smallest dimensional features such as the gate length in FET devices or the emitter width in bipolar devices. Table 3 lists most of the commercially available MMIC foundries worldwide. Many other foundries, not listed in Table 3, are either R&D facilities or offer their manufacturing capabilities only to their internal

corporate customers or serve their own line of products. Only Gallium Arsenide (GaAs) and Silicon foundries are available for large scale MMIC production, other semiconductors are used in research labs or in small foundries that are mainly engaged in advancing the state-of-the-art.

When MMIC technology was being developed mainly through government funds in mid 1980s till mid 1990s, MMIC manufacturers had small facilities but today the most successful foundries are much larger. It is estimated that a new MMIC foundry needs investments of at least $200 - $500 million. In selecting a foundry process the cost per mm^2 of wafer should be the driving factor to remain competitive and for this reason many foundries are upgrading their equipment to 6" GaAs wafers to lower the cost to their customers. The cost of a MMIC chip is very low and can vary from $0.20 to $3.0 per mm^2 depending on the size of the chip and the process used in manufacturing. SiGe MMICs are the cheapest while 0.15µm pHEMT, GaN HEMT and SiC Mesfet are the most expensive. MMIC development is costly and time consuming; the cost of a foundry run can vary from $40,000 to $100,000 depending on process type, number of wafers requested and any post fabrication steps requested such as on-wafer testing or pick-and-place. The cost usually includes a complete set of masks (usually 8 to 15 layers) and 2 to 6 diced wafers ready for pick and place. Few foundries such as WIN Semiconductors and Triquint offer arrangements for their customers to share the masks or offer lower costs during initial development runs.

Table 3: List of MMIC Foundries Worldwide

Foundry	Location	Capabilities	Processes offered	Market
Cree	Durham, NC, USA	3" SiC & GaN	GaN HEMT & SiC Mesfet	Offers SiC foundry services & has a product line
Filtronics Compound Semiconductors	Santa Clara, CA, USA	6" GaAs	0.2µm pHEMT	Offers foundry services & has a product line
GCS	Torrance, CA, USA	6" GaAs	0.5µm pHEMT, InGaP & InP HBT	Only offers foundry services
IBM	Burlington, VT, USA	Silicon	0.18µm,0.25µm,0.35µm,0.5µm SiGe BiCMOS & 0.13µm, 0.18µm,0.25µm RFCMOS	Only offers foundry services
Knowledge ON	Iksan, S. Korea	6" GaAs	InGaP HBT	Offers foundry services & has a product line
M/A COM	Lowell, MA & Roanoke, VA, USA	4" GaAs	0.18µm ,0.5µm & 1µm pHEMT,0.5µm & 1µm Mesfet, MSAG	Offers foundry services & has a product line
Nitronex	Raleigh, NC, USA	GaN on 4" Silicon	GaN HEMT	Offers new foundry services & has a product line
SiGe Semiconductor	Ottawa, Ontario, Canada	SiGe	SiGe BiCMOS	Offers foundry services & has a product line
Transcom	Tainan, Taiwan	6" GaAs	0.25µm & 0.5µm PHEMT, HFET & MESFET	Offers foundry services & has a product line
Triquint Semiconductor	Portland, OR & Dallas, TX, USA	6" GaAs & GaN	0.15µm MHEMT, 0.13µm, 0.25µm,0.35µm, 0.5µm pHEMT, 0.5µm & 0.6µm Mesfet, 0.5µm HFET,3µm InGaP HBT	Offers foundry services & has a product line
United Monolithic Semiconductor	Ulm, Germany Orsay, France	4" GaAs	0.15µm, 0.25µm pHEMT and 2µm HBT	Offers foundry services & has a product line
WIN Semiconductor	Tao Yuan Shien, Taiwan	6" GaAs	0.15µm, 0.5µm pHEMT and 1µm , 2µm HBT	Only offers foundry services

MMIC Chips are small and fragile and most microwave and communications companies do not have the special equipment to handle MMIC chips such as pick-and-place machinery, die attach or wire bonding., therefore packaging a MMIC is usually needed before insertion in any system or sub-system application. MMIC packages vary in shapes, dimensions and number of pins and packaging and assembly could be a major cost unless the process is fully automated. Most cheap package types have serious limitations at high frequencies (> 5GHz). MMICs are packaged either directly on carriers such in Fig. 4 or in specially designed packages such as drop-in packages or Surface Mount Technology (SMT) packages (Fig. 5a, b, c).

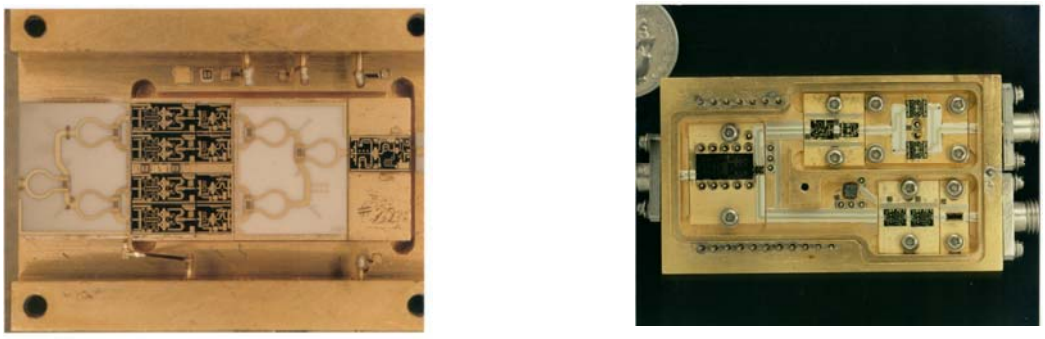
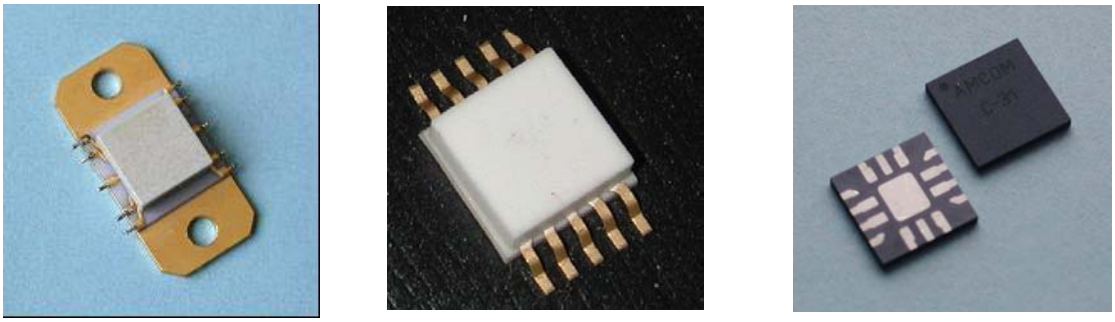


Figure 4: Examples of Carrier Mounted MMICs

High frequency packages such as in Fig. 5a & b are made of co-fired ceramic with an internal cavity to attach the MMIC to the metal using epoxy or solder. The ceramic or plastic lid is usually attached to the cavity using epoxy. Most low cost packages such as in Fig. 5c use plastic encapsulation on lead frames.



a) Ceramic Drop-in Package b) SMT Ceramic Package c) SMT Plastic Package

Figure 5: Examples of MMIC Packages

IV. MMIC DESIGN GUIDELINES

The RF designer most important task is to meet his RF and packaging specifications but other important factors are sometimes overlooked when designing a new MMIC. The most important step is to choose the semiconductor process best suited for the application at hand. Each combination of frequency and application type such as PA, LNA or switching would use a different process as suggested in Table 2. Besides selecting a suitable MMIC process, the RF designer should verify his device models, select device sizes, choose and simulate several circuit configurations, minimize chip size during layout, make chip yield estimates, perform thermal analysis and select the best MMIC package assembly technique. Figure 6 shows a block diagram of the different steps needed to produce a MMIC prototype and Figure 7 summarizes the steps for taking a MMIC design from a prototype phase into production.

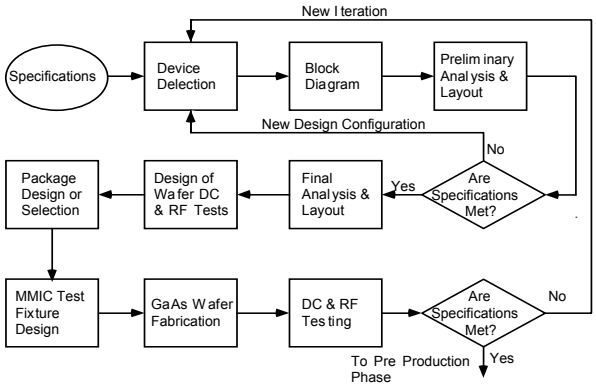


Figure 6: Block Diagram of MMIC development phase

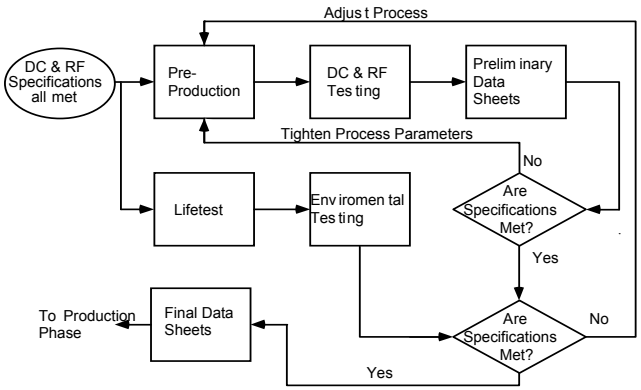


Figure 7: Block Diagram of MMIC production phase

Few design considerations are discussed below:

a) Device Characterization

Most foundries offer active device models but it is unfortunate that some of these published models are not accurate therefore the designer may need to spend a significant amount of time to characterize sample devices. Small signal S-parameters measurements are always a must at different device bias voltages and currents. If the MMIC application is for power application the device should be characterized using Load-Pull setup that measure output power at 1dB compression (P_{1dB}) saturated power (P_{sat}), efficiency (η) and linearity (IMD, EVM …etc). Efficiency and linearity are always difficult to achieve simultaneously. If the application is for low noise a Source-Pull measurement should be performed to find the best input impedance for low noise. The devices used for characterization do not need to be the same periphery (i.e. total gate or emitter periphery) used in the design since microwave devices could easily be scaled. Several devices should be characterized from different wafers and from different wafer runs to ensure that the designer has a grasp on the variations in device parameters across a single wafer, from wafer to wafer and from run to run. Device characterization could easily account for 50% of the design time but it is time well spent otherwise the consequences could be additional iterations, extended design cycle and cost.

c) Device Scaling

The device size used for a particular application is dictated by the RF specs such as power and the matching requirement. For most MMIC applications the active device is chosen to have input and output impedances that can easily be matched to 50 Ohms which is the characteristic impedance of all microwave interconnects and systems at microwave frequencies. This is the fundamental reason MMICs could not be made smaller as predicted by Moore's law for digital circuits. The devices that are available for characterization by a foundry are usually small devices (0.3 to 2mm) and the designer does not have the luxury to measure the exact device size he selects for his design. However, the S-parameters, Load-Pull and Source-Pull data are easily scaled to the proper size. To illustrate how you could scale a device consider the following example. If a device under characterization has 1mm periphery, delivers 0.4W of optimum power into an output load of 30+j20 Ohms load at 45% efficiency and has an optimum noise figure of 3dB with an input source impedance of 10+j10 Ohms at 5GHz, a 2mm device (factor of 2 larger) would deliver 0.8W of optimum power into an output load of 15+j10 Ohms load at 45% efficiency and should have a minimum noise figure of 3dB with an input source impedance of 5+j5 Ohms at the same frequency. If a small equivalent circuit is derived then all admittance parameters such as capacitors, trans-conductance become proportional to the size and all impedance parameters such as resistors and inductances are inversely proportional to the device size.

It is critical when scaling a device to keep gate or emitter fingers geometry the same since changing the geometry would lead to scaling error. Also the device input and output pads and location of via holes to ground should be properly modeled during design. It is recommended to keep device length and size less than 5% of a wave length to avoid having different parts of the device being out of phase. In case of power applications requiring large devices the designer should combine several device cells of reasonable size using common combining techniques.

d) Circuit design and Simulation

A MMIC design should be based on the simplest possible configuration meeting the RF specs in order to keep the size of the MMIC as small as possible and to avoid simulation errors due to design complexity. Most simulation predictions differ from actual measurements for variety of reasons and the simpler the design less variations would occur. Some of the factors affecting simulation inaccuracies are: EM coupling, which could be minimized by leaving at least one substrate height gap between elements, the use of non-standard library elements, layout errors, process variations and modeling errors. A robust MMIC design should be simple, with no coupling between elements, and should still meet the RF specification with capacitance and resistor variations of at least ±10%. The circuit configuration is always limited by the Bode-Fano theorem which states that matching of any impedance with resistive and reactive components is bandwidth limited [19]. The most common technique that should be used in case of a large bandwidth requirement is to use resistive elements at the input or output of a transistor or add resistive feedback. For a power or low noise MMIC this may not be an option since a resistive network at the output would be too lossy and for an LNA the input loss could degrade the noise figure.

e) Chip Yield

The cost of a MMIC chip is inversely proportional to chip yield which is a function of die size and wafer defects density as shown in the following formula in reference [1] on p. 61:

$$\text{Yield} = \exp(-A_g D_g - A_c D_c)$$

$$\text{Chip Cost} = (\text{Wafer Cost}/\text{Wafer Area}) \cdot A_m \cdot \exp(A_g D_g + A_c D_c)$$

A_g is the device gate or emitter area and D_g is the average lattice defect density
A_c is the capacitor area and D_c is the capacitor defect density
A_m is the MMIC area

Note that the yield decreases exponentially with device periphery and total MMIC capacitor sizes and consequently cost will go up also exponentially. This is why power applications where devices are relatively large are the most demanding applications and are also the most expensive MMICs. Yield of power devices is also a major limitation on the maximum

power that a MMIC could deliver. A GaAs MMIC maximum size is usually limited to 10 to 20 mm^2. For very low cost MMIC the size is usually under 2 to 3 mm^2.

f) Thermal Analysis

Thermal analysis is a must particularly if the design uses large periphery devices. The junction temperature of the device should never exceed the maximum recommended temperature of the selected process to guarantee reliable operation. The analysis should take into account the maximum ambient temperature, the temperature rise in the MMIC package and the PCB in SMT applications. Usually GaAs FETs used for consumer MMICs could tolerate a junction temperature up to 175°C but for high reliability applications 120°C may be necessary.

V. MMIC Surveys and Examples of Novel MMIC Circuits

In this section a brief survey of MMIC amplifiers is presented since amplifiers have demanding requirements and their design is more challenging than passive applications. Fig. 8 presents a recent literature survey of major accomplishments in power MMIC design by MMIC category. Notice that although GaN and LDMOS MMICs are new, they give the highest powers compared to other technologies. From the number of GaAs FET MMICs it is obvious that they are the most popular to date but GaAs HBT MMICs are being used mainly in the cellular and wireless band applications because of their low cost and superior efficiency. Fig. 9 shows a similar survey for low noise MMICs, notice again that the GaAs FET is dominating low noise applications below 100GHz and InP is the only candidate for applications above 100GHz. The power of each particular technology such as LDMOS, GaAs follows the famous $P_{max}f^2$ = Constant law which states that the maximum power a particular technology offers, P_{max} , is proportional to $1/f^2$. The P_{max} f^2 constant varies with different technologies it is highest for SiC and lowest for InP. If a scaling of this P_{max} f^2 constant is made we could rank the different technologies in descending order as follows: SiC MESFET, GaN HEMT, LDMOS, GaAs FET, GaAs HBT and finally InP. Novel techniques were introduced to raise the power capability in GaAs such the field plate concept [20] and the HiFET circuit configuration [21]. Figure 10 shows the HiFET concept which is applicable to any FET technology and can help generate power levels not possible with single devices. Figure 11 shows an actual implantation of a HiFET MMIC with 3 W of output power over 0.05 to 3GHz.

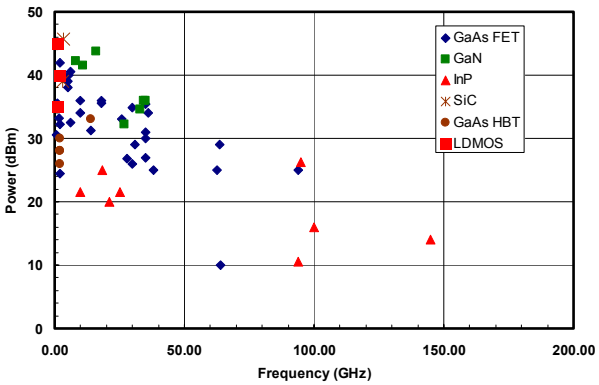


Fig. 8: Power MMIC Survey

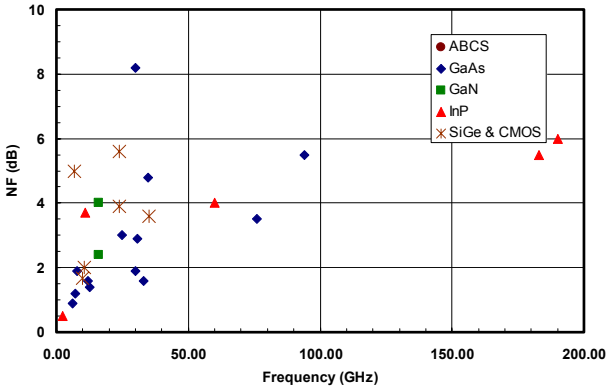


Fig. 9: LNA MMIC Survey

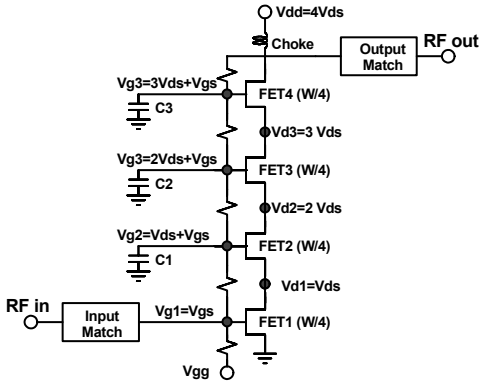


Figure 10:HiFET Concept Configuration

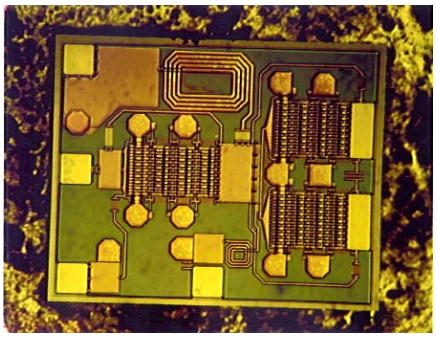


Figure 11: 3Watt Broadband MMIC using HiFET

Three-dimensional (3-D) MMICs are gaining attention for compact designs and potential applications at mm-wave [22-23]. 3-D MMICs are particularly useful at mm-wave where thin substrates are needed to avoid coupling between elements and also help overcome the loss of the Silicon substrate in BiCMOS.

VI. Conclusion and Future Trends

GaAs MMIC technology is currently mature enough to have a dominant presence for power, low noise and passive applications from few GHz to 100GHz. Improvement in power levels, efficiency and linearity for GaAs PA applications will continue to happen in the next few years particularly for HBT MMIC which is the main player in cellular and wireless applications. GaAs MMIC technology is not suitable for integrating digital and analog functions and BiCMOS MMICs will start to satisfy the need of mixed signal and system on a chip applications (SOC), however, BiCMOS will have difficulty competing with the established GaAs chips at the 1 to 10W power levels and in very low noise applications (i.e. NF < 1dB). For power levels above 10W, the new technologies based on GaN will start filling the gap in power applications in the 10W to 100W up to mm-wave. SiC and LDMOS technologies would continue to produce >10W MMICs for applications below 5GHz but are not expected to compete with GaN or GaAs at higher frequencies. Power dissipation of high power MMICs will necessitate the use of flip-chip designs to lower device junction temperature. InP will dominate the mm-wave above 100GHz. Three dimensional MMICs will see further developments to achieve higher level of integrations particularly in SiGe and will find a niche application at mm-wave frequencies.

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