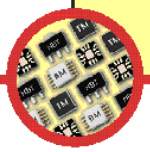
Gallium Nitride MMIC 15W 3.75 – 8.25 GHz Power Amplifier

AM408041WN-00-R
AM408041WN-SN-R
November 2017
P1



DESCRIPTION

AMCOM's AM408041WN-00 Chip is a broadband GaN MMIC power amplifier. It has 33dB gain, and 42 dBm output power over the 3.75 to 8.25 GHz band. The AM408041WN-SN-R is in a ceramic package with a flange and straight RF and DC leads for drop-in assembly. It has 31dB gain, and 41.5 dBm output power over the 3.75 to 8.25 GHz band. Because of high DC power dissipation, good heat sinking is required. The package is RoHS compliant. This MMIC is matched to 50 Ohms.

FEATURES

- Broadband from 3.75 to 8.25GHz
- Saturated output power Psat is 41.5dBm
- High gain, 31dB
- Input & output DC blocked and matched to 50 Ohms

APPLICATIONS

- Instrumentation
- Commercial telecom transmission equipment
- Fixed microwave backhaul

TYPICAL PERFORMANCE (AM408041WN-00-R Chip Data)

Parameters	Minimum	Typical **	Maximum
Frequency	4-8 GHz	3.75-8.25 GHz	
Small Signal Gain	29dB	33dB	
Gain Ripple		± 2dB	± 4.0dB
P1dB	35dBm	38dBm	
Psat	39dBm	42dBm	
Psat Efficiency		26%	
Noise Figure		TBD (TBD)	
IP3		TBD (TBD)	
Input Return Loss	10 dB	15dB	
Output Return Loss		5dB	
Thermal Resistance		TBD	

* Specifications subject to change without notice.

** Bias Conditions**: $V_{ds1,\,2,\,3}$ = +28V, I_{dsq1}+ I_{dsq2} = 0.65A, I_{dsq3} = 0.90A, V_{gs1} = V_{gs2} = V_{gs3}=-1.8V.

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TYPICAL PERFORMANCE (AM408041WN-SN-R Packaged Data)

Parameters	Minimum	Typical **	Maximum
Frequency	4-8 GHz	3.75-8.25 GHz	
Small Signal Gain	26dB	31dB	
Gain Ripple		± 2dB	± 4.0dB
P1dB	34.5dBm	37.5dBm	
Psat	38.5dBm	41.5dBm	
Psat Efficiency		23%	
Noise Figure		TBD (TBD)	
IP3		TBD (TBD)	
Input Return Loss	10 dB	15dB	
Output Return Loss		5dB	
Thermal Resistance		TBD	

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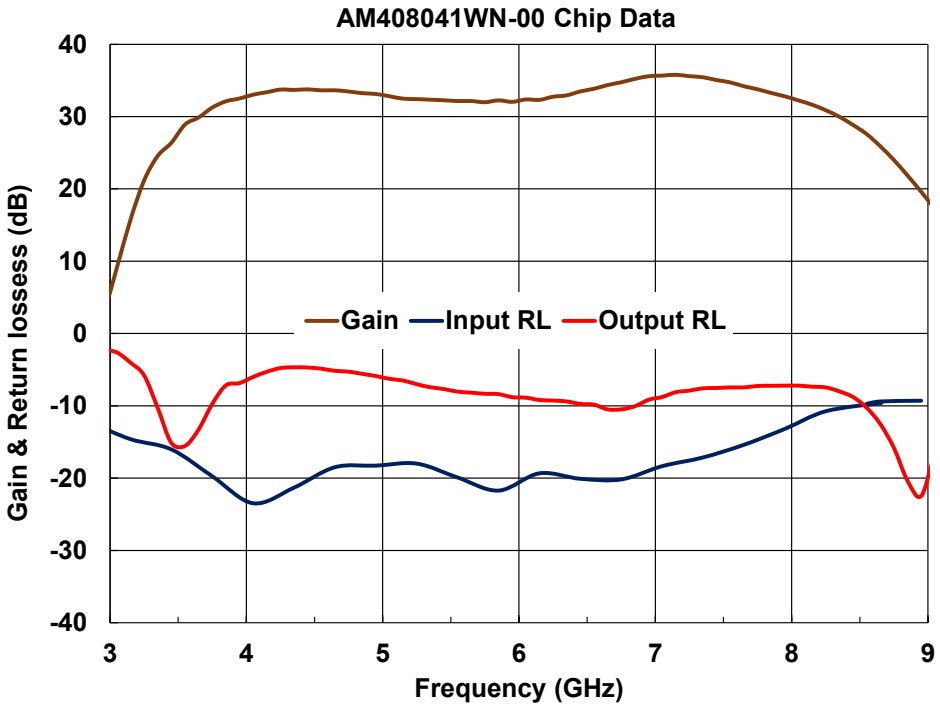
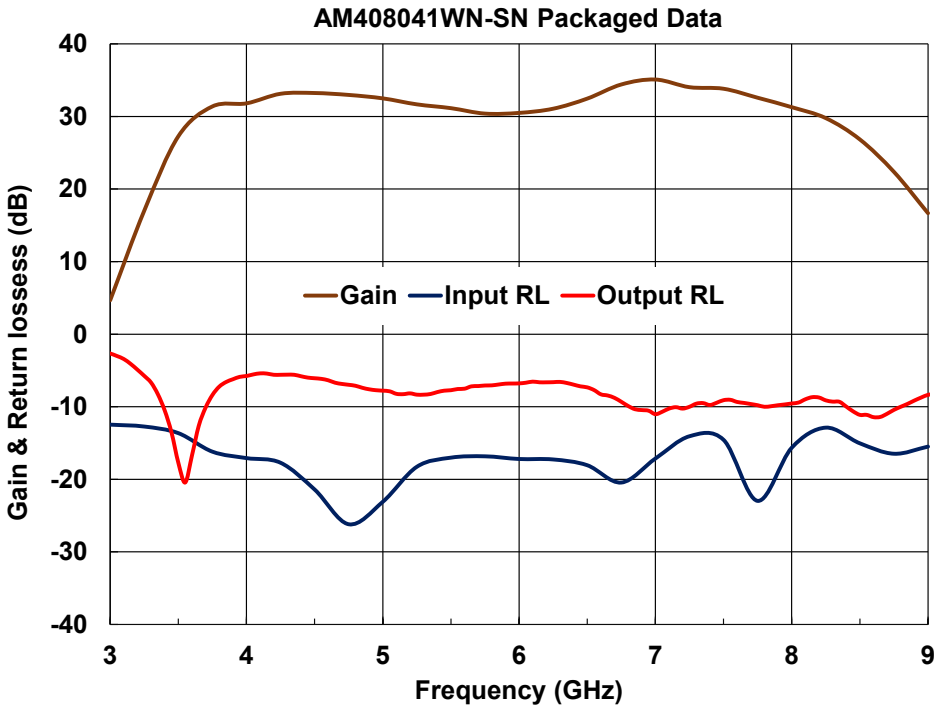
** Bias Conditions**: $V_{ds1,\ 2,\ 3}$ = +28V, I_{dsq1}+ I_{dsq2} = 0.65A, I_{dsq3} = 0.90A, V_{gs1} = V_{gs2} = V_{gs3}=-1.8V.

ABSOLUTE MAXIMUM RATING

Parameters	Symbol	Rating
First & second stage drain voltages	V_{ds1} , V_{ds2}	36V
Second stage drain voltage	V_{ds3}	36V
Gate source voltage	V_{gs1}, $V_{gs2,\ Vgs3}$	-6V
Drain source current	I_{dsq1} + I_{dsq2}	1A
Drain source current	I_{dsq3}	1.5A
Continuous dissipation at 25ºC	P_t	100W
Channel temperature	T_{ch}	200°C
Operating temperature	T_{op}	-55°C to +85°C
Storage temperature	T_{sto}	-55°C to +135°C

SMALL SIGNAL DATA*





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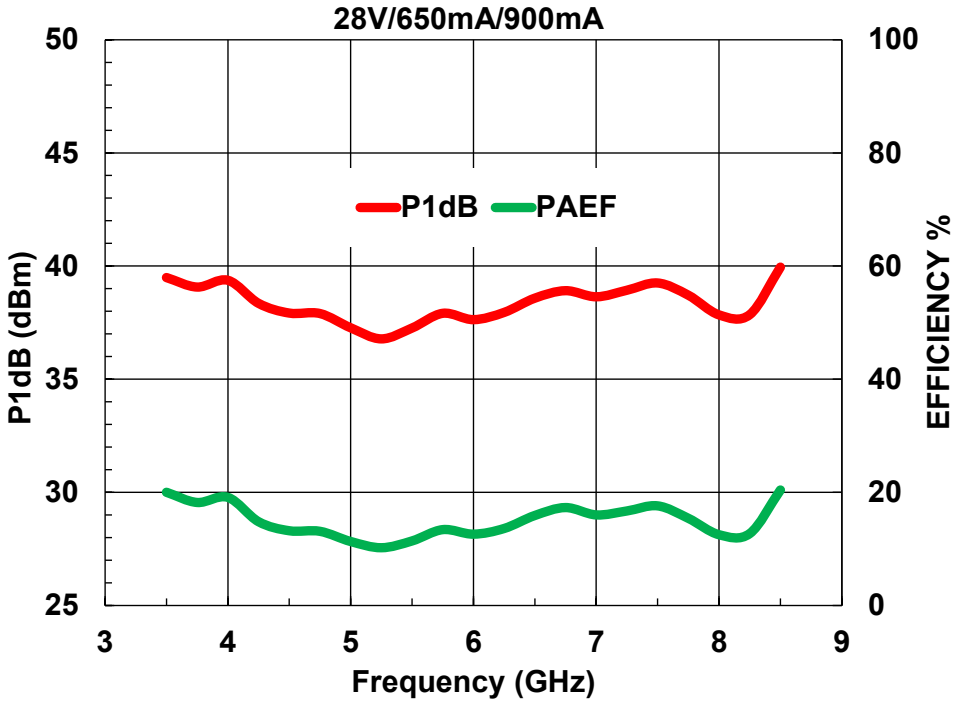
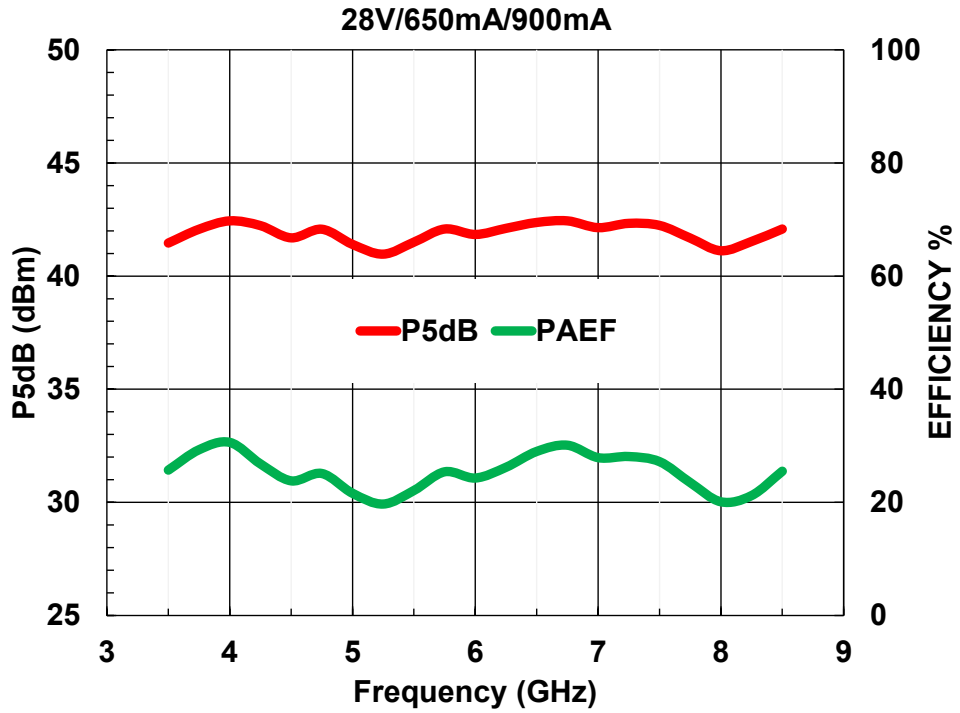
POWER DATA**

A) AM408041WN-00-R Chip Data





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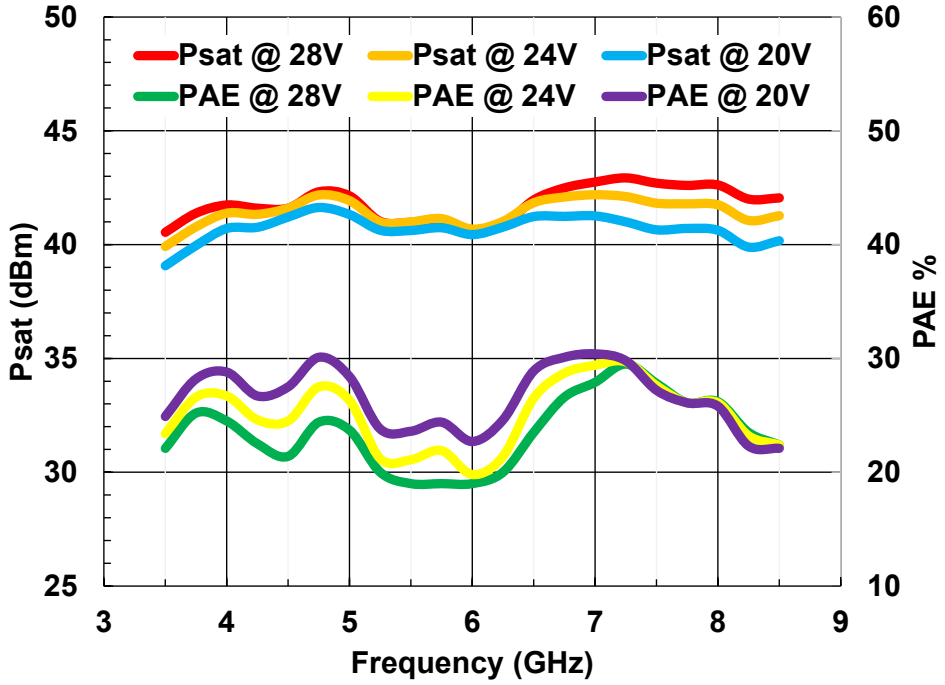
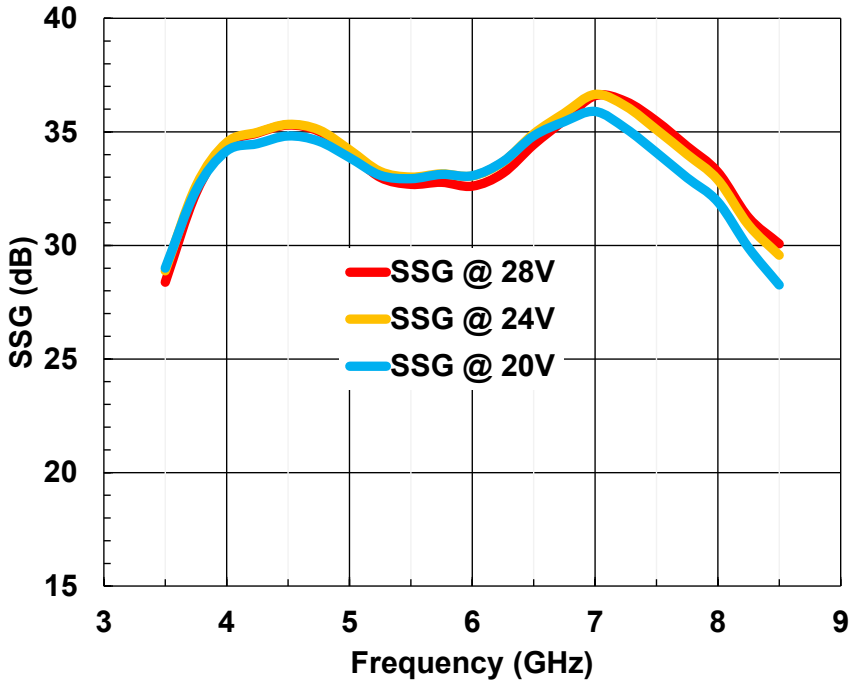
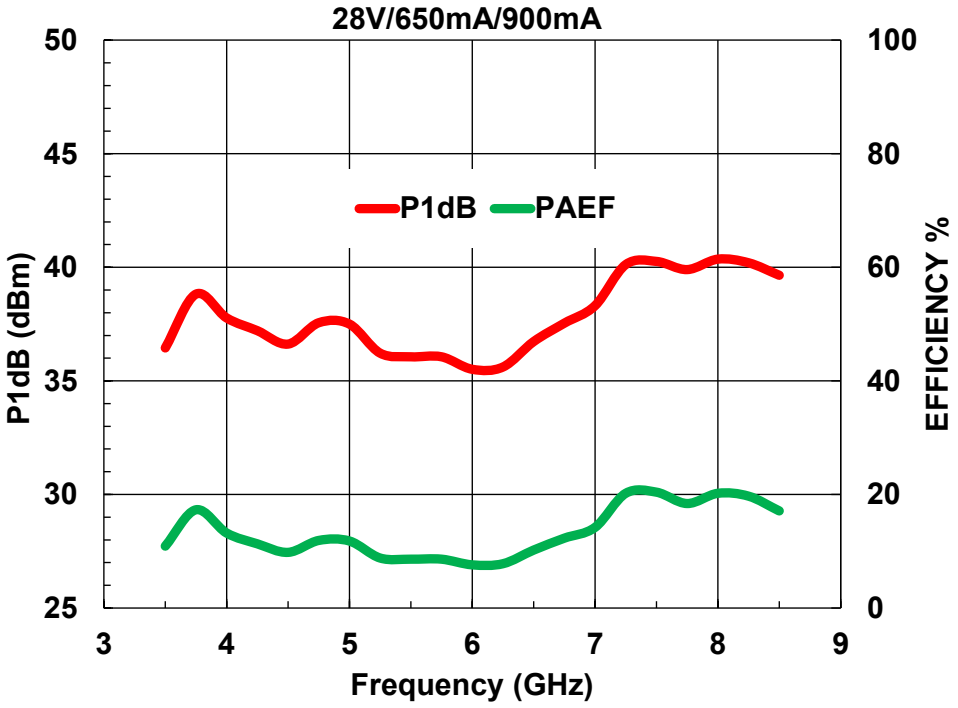
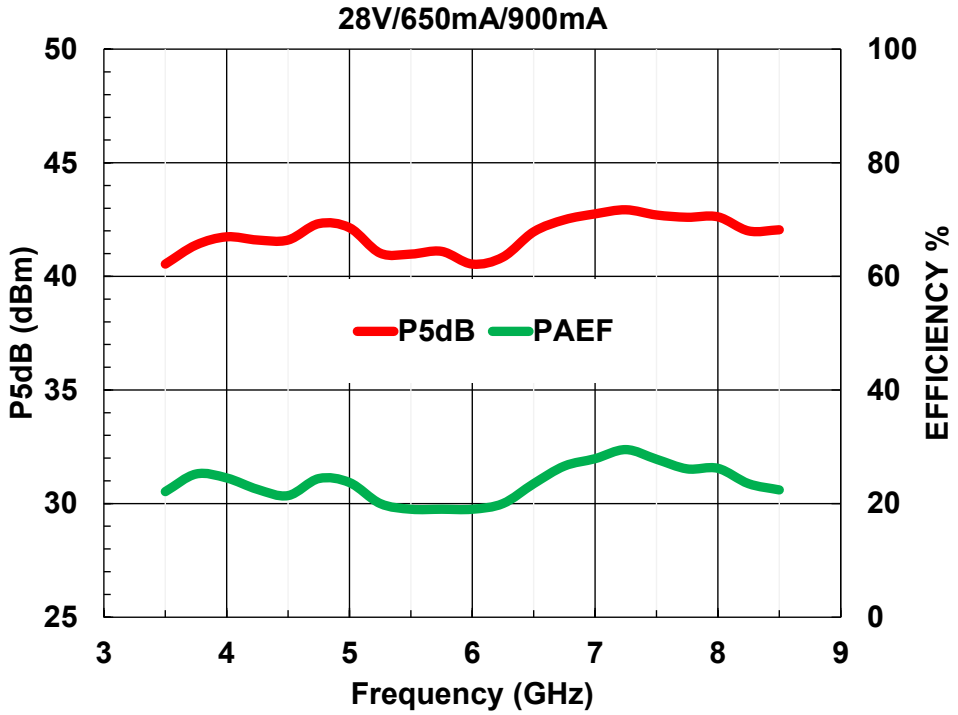
B) AM408041WN-00-R Chip Data at different V_{dd}





C) AM408041WN-SN-R Packaged Data





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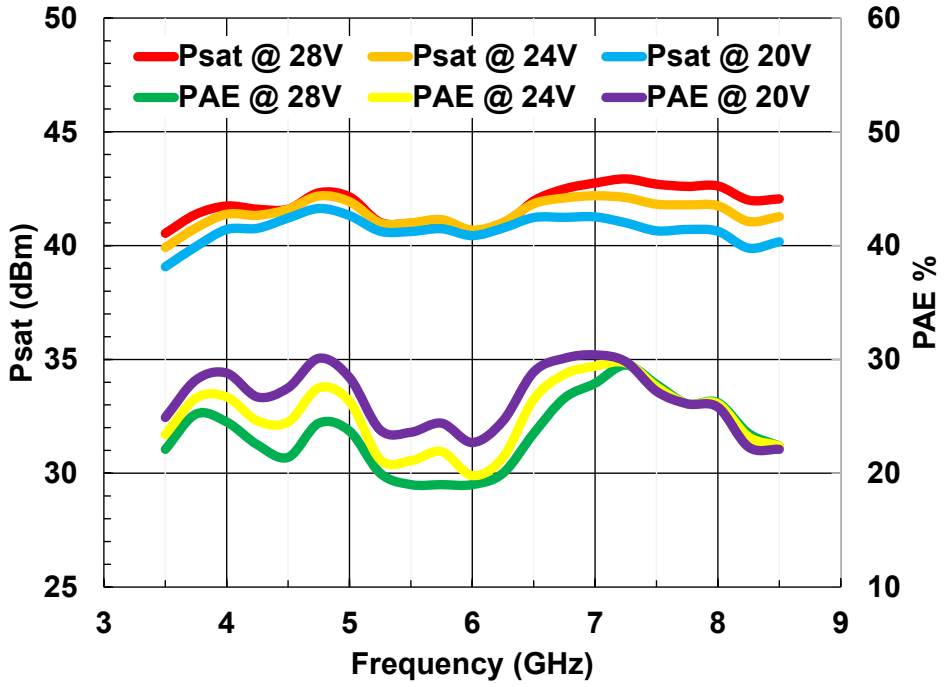
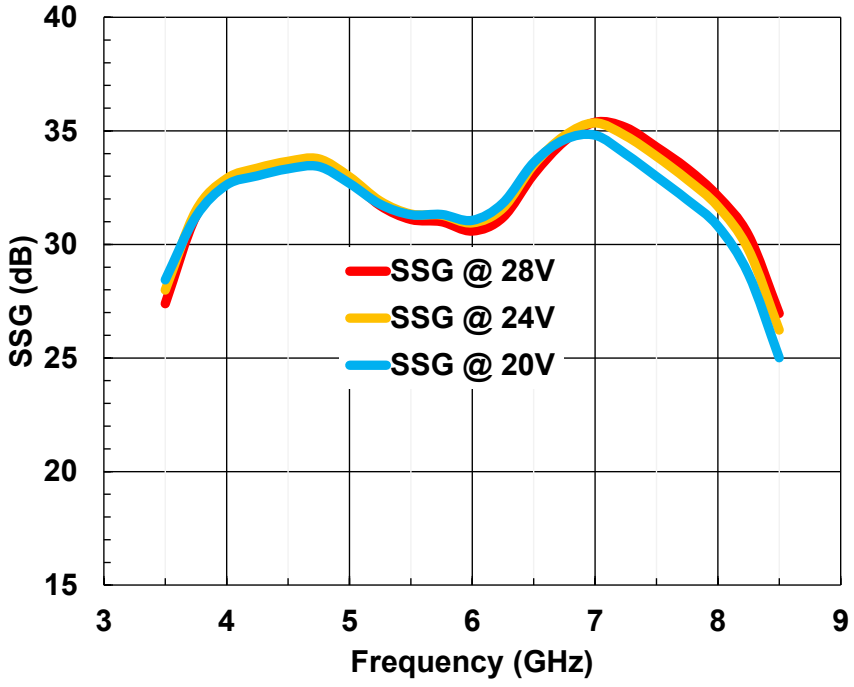
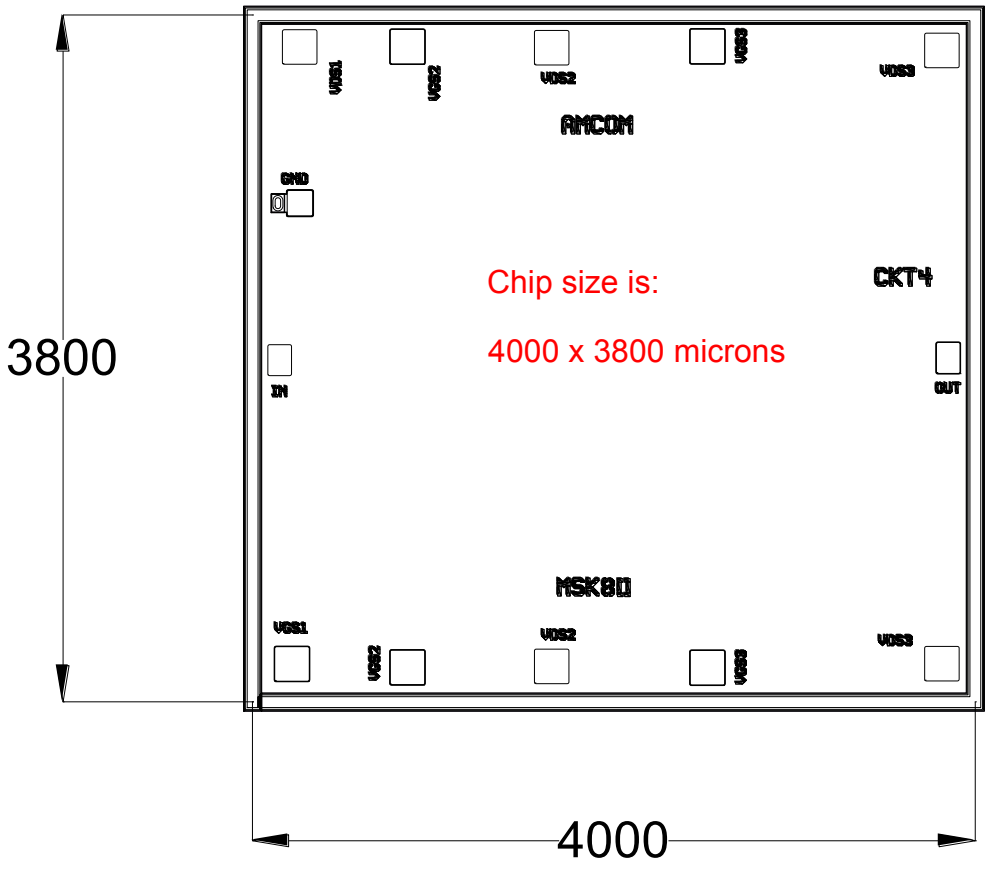
D) AM408041WN-SN–R Packaged Data at different V_{dd}





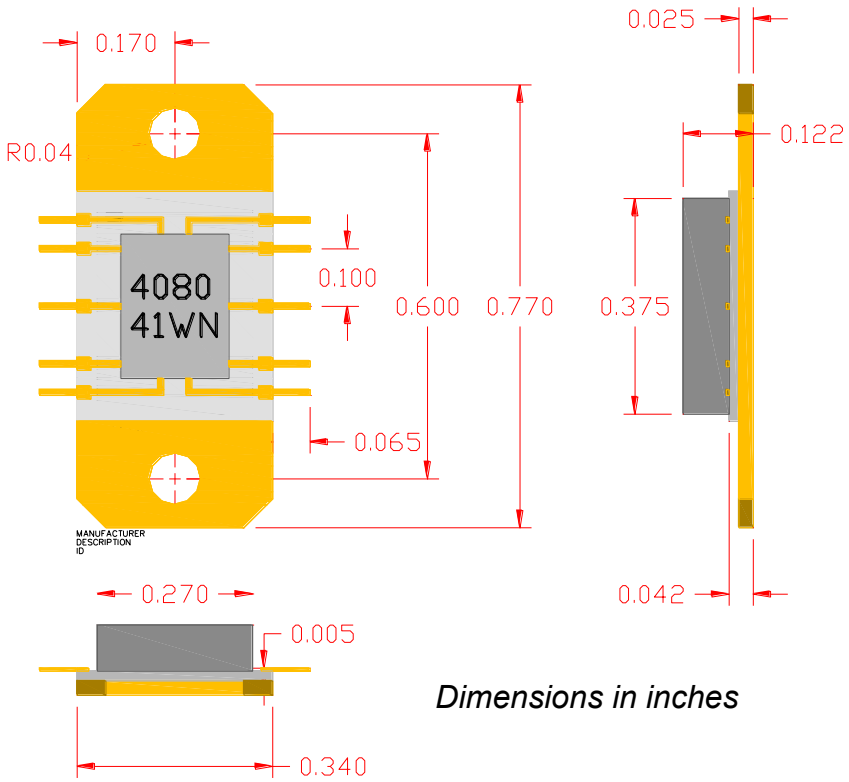
CHIP OUTLINE



Notes:

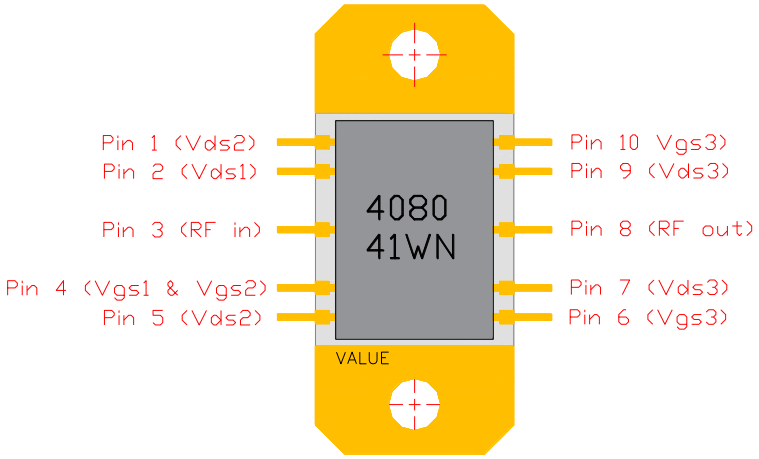
1) RF bond pads are 140X180 microns, 50 ohm matched and DC blocked.
2) Drains and Gates pads are all 200x200 microns
3) Use eutectic perform for ship assembly

PACKAGE OUTLINE



Dimensions in inches

Pin Layout



Pin No.	Function	Bias
1	Vds2	+28V
2	Vds1	+28V
3	RF in	-
4	Vgs1 & Vgs2	-1.8V
5	Vds2	+28V
6	Vgs3	-1.8V
7	Vds3	+28V
8	RF out	-
9	Vds3	+28V
10	Vgs3	-1.8V

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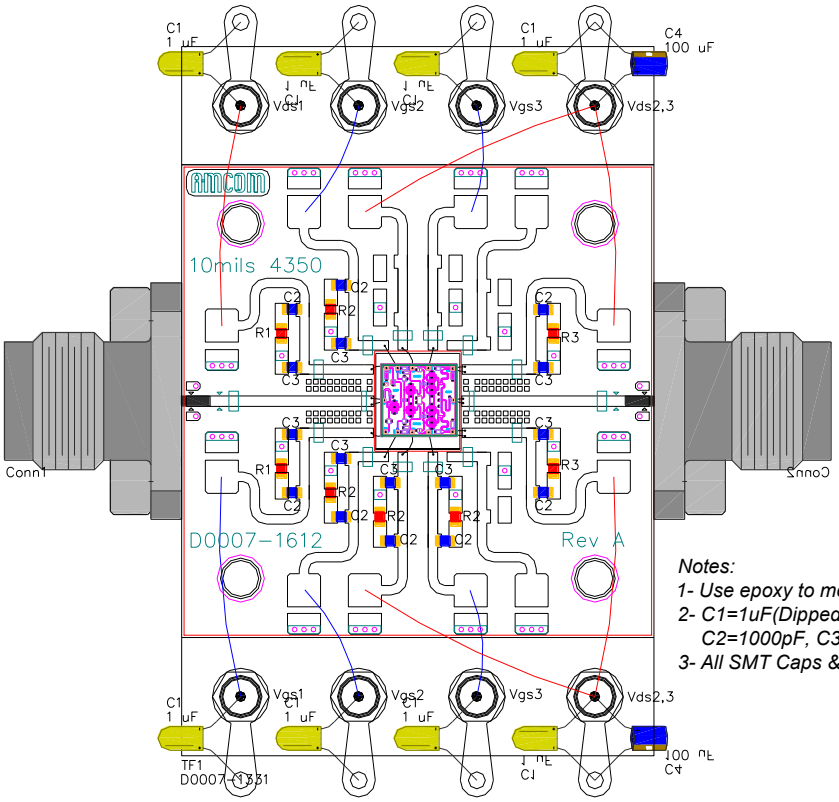
TEST CIRCUIT (Chip Version)



Notes:
1- Use epoxy to mount PCB, and Eutectic soldering to mount chip
2- C1=1uF(Dipped Radial Tantalum),C4=100uF(Aluminum Electrolytic)
C2=1000pF, C3=20pF , R1=50ohms, R2=10ohms, R3=5ohms
3- All SMT Caps & Resistors are 0402 size

Important Notes:

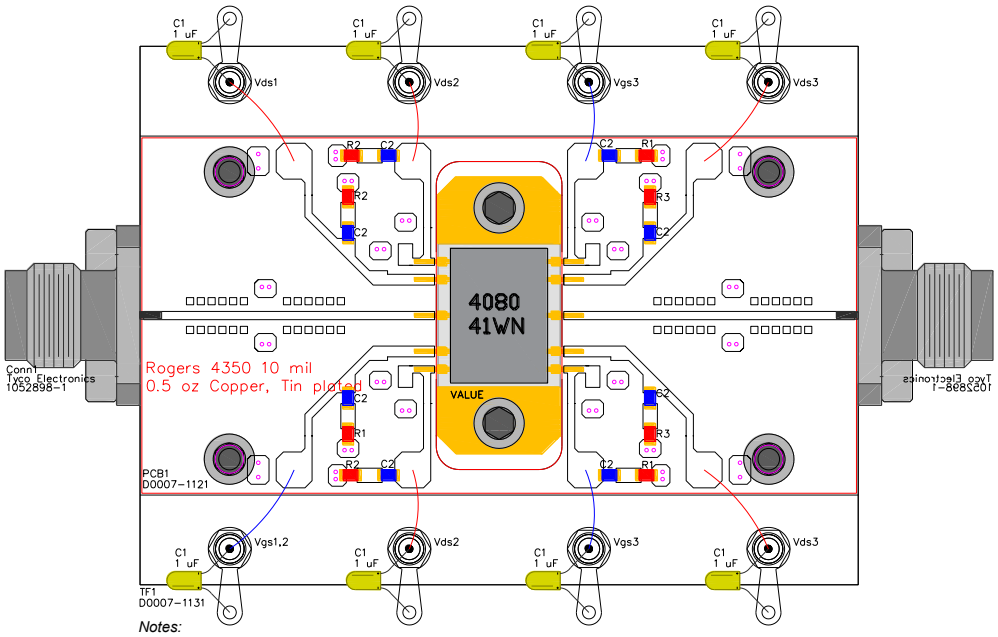
1- Recommended current biases are 220mA for first, 430mA for second stage and 900mA for the third stage. Gate biases of 1.8V are for reference only. Gate voltages could be adjusted to vary the currents going thru drain pins.

2- Do not apply drain voltages without proper negative voltages on gates. Otherwise MMIC would fail due to excess heat.

3- Eutectic soldering is recommended for chip mounting

4- AutoCAD DXF file is available

TEST CIRCUIT (Packaged Version)



Notes:
1- Use epoxy to mount PCB
2- C1=1uF, C2=1000pF, R1=50ohms, R2=10ohms, R3=5ohms
3- All SMT Caps & Resistors are 0603 size
4- Use Test Block No. D0007-1131

Important Notes:

1- Recommended current biases are 650mA for first and second stage combined and 900mA for the third stage. Gate biases of 1.8V are for reference only. Gate voltages could be adjusted to vary the currents going thru drain pins.

2- Do not apply drain voltages without proper negative voltages on gates. Otherwise MMIC would fail due to excess heat.

3- AutoCAD DXF file is available