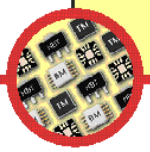
Gallium Nitride MMIC 12W 2.0 – 6.0 GHz Power Amplifier

AM206041WN-SN-R
July 2017
Preliminary



DESCRIPTION

AMCOM's AM206041WN-SN-R is a broadband GaN MMIC power amplifier. It has 30dB gain, and 41 dBm output power over the 1.8 to 6.5GHz band. The AM206041WN-SN-R is in a ceramic package with a flange and straight RF and DC leads for drop-in assembly. Because of high DC power dissipation, good heat sinking is required. The package is RoHS compliant. This MMIC is matched to 50 Ohms.

FEATURES

- Broadband from 2.0 to 6.5GHz
- Saturated output power Psat is 41dBm
- High gain, 26dB
- Input & output matched to 50 Ohms

APPLICATIONS

- Instrumentation
- Commercial telecom transmission equipment
- Fixed microwave backhaul

TYPICAL PERFORMANCE *

Parameters	Minimum	Typical **	Maximum
Frequency	2.5 – 6.0GHz	1.8 – 6.5GHz	
Small Signal Gain	25dB	30dB	33dB
Gain Ripple		± 2dB	± 5.0dB
P1dB	36dBm	38dBm	
Psat	39dBm	41dBm	
Psat Efficiency		20%	
Noise Figure		TBD	
IP3		TBD	
Input Return Loss	10dB	>14dB	
Output Return Loss	3dB	>5dB	
Thermal Resistance		TBD	

* Specifications subject to change without notice.

** Bias Conditions: V_{ds1} = V_{ds2} = +28V, I_{dsq1} + I_{dsq2} = 0.6A, V_{gs1} & V_{gs2}=-2.0V, V_{ds3} = +28V, I_{dsq3} = 0.9A, V_{gs3}=-2.0V
Gate biases may change from chip to chip to get the specified currents

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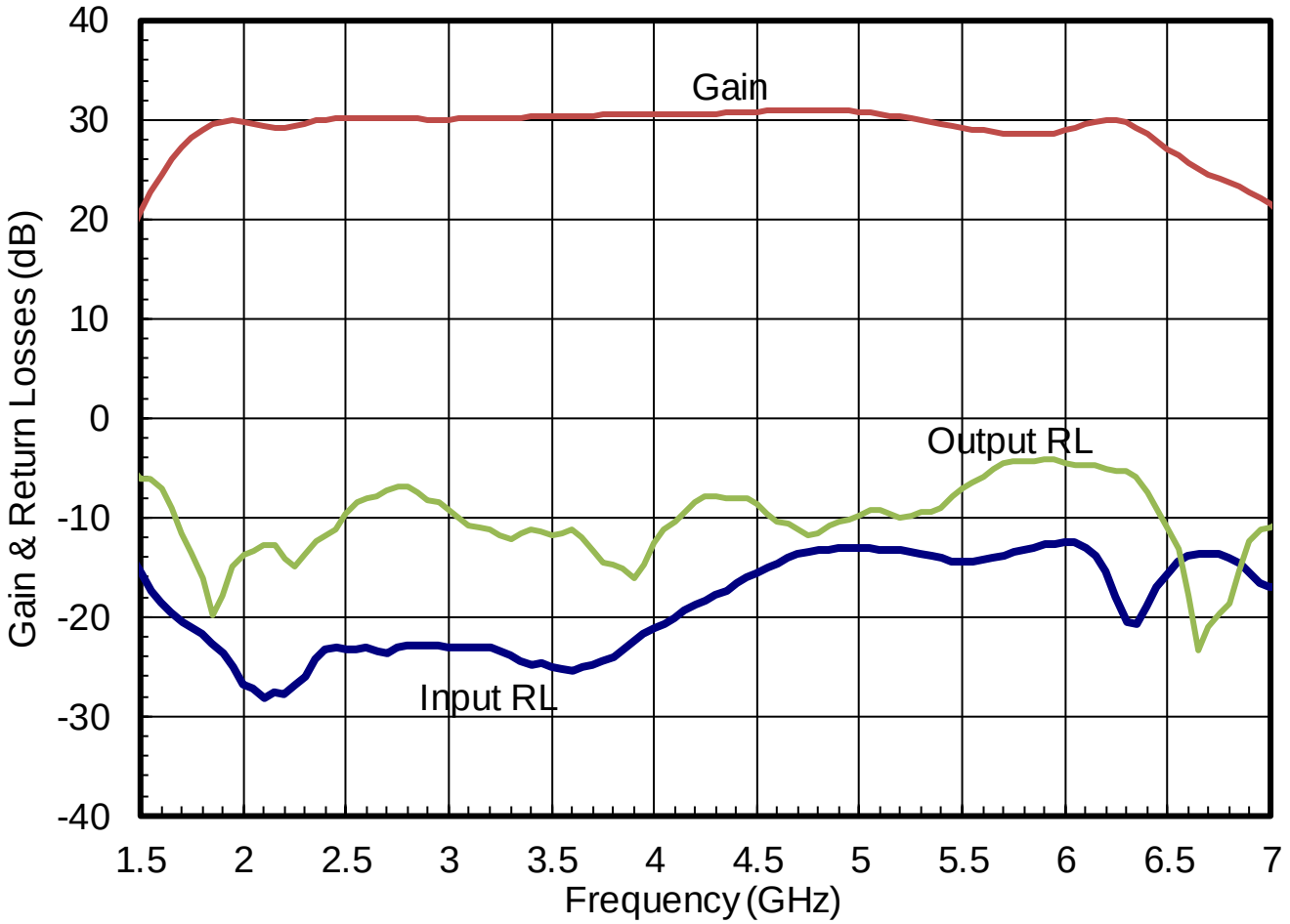
401 Professional Drive, Gaithersburg, MD 20879

ABSOLUTE MAXIMUM RATING

Parameters	Symbol	Rating
First & second stage drain voltages	V_{ds1} , V_{ds2}	35V
Second stage drain voltage	V_{ds3}	35V
Gate source voltage	V_{gs1}& V_{gs2}	-6V
Drain source current	I_{dsq1} + I_{dsq2}	0.75A
Drain source current	I_{dsq3}	1.1A
Continuous dissipation at 25ºC	P_t	80W
Channel temperature	T_{ch}	200°C
Operating temperature	T_{op}	-55°C to +85°C
Storage temperature	T_{sto}	-55°C to +135°C

SMALL SIGNAL DATA*



* S-Parameters measured using test fixture. Bias is $V_{ds1} = V_{ds2} = V_{ds3} =$ 28V , $I_{ds1} + I_{ds2}$=600mA , I_{ds3}=900mA , $V_{gs1} = V_{gs2} = V_{gs3}$ =-2.0V .

NOISE DATA

(TBD)

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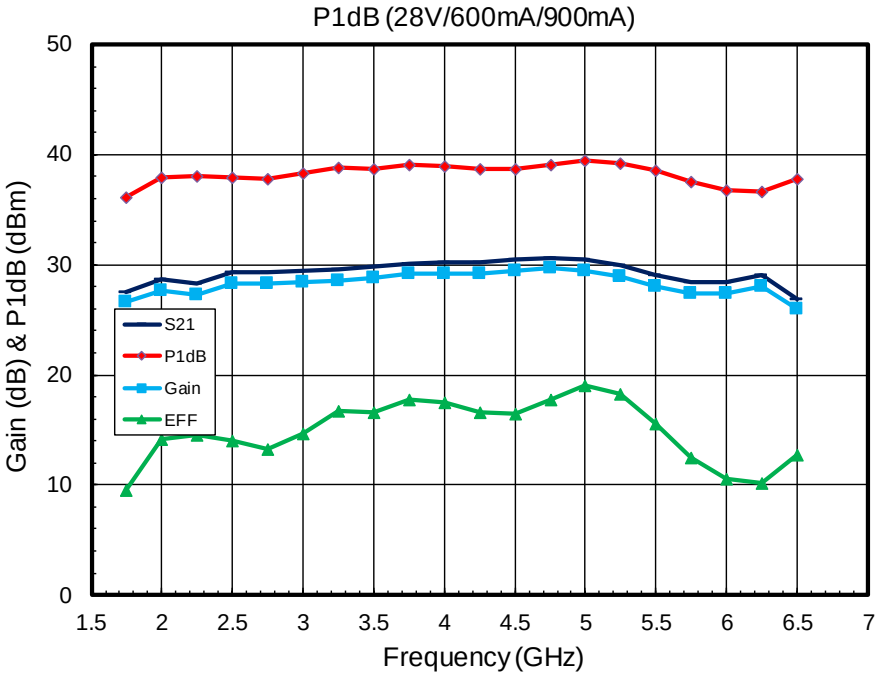
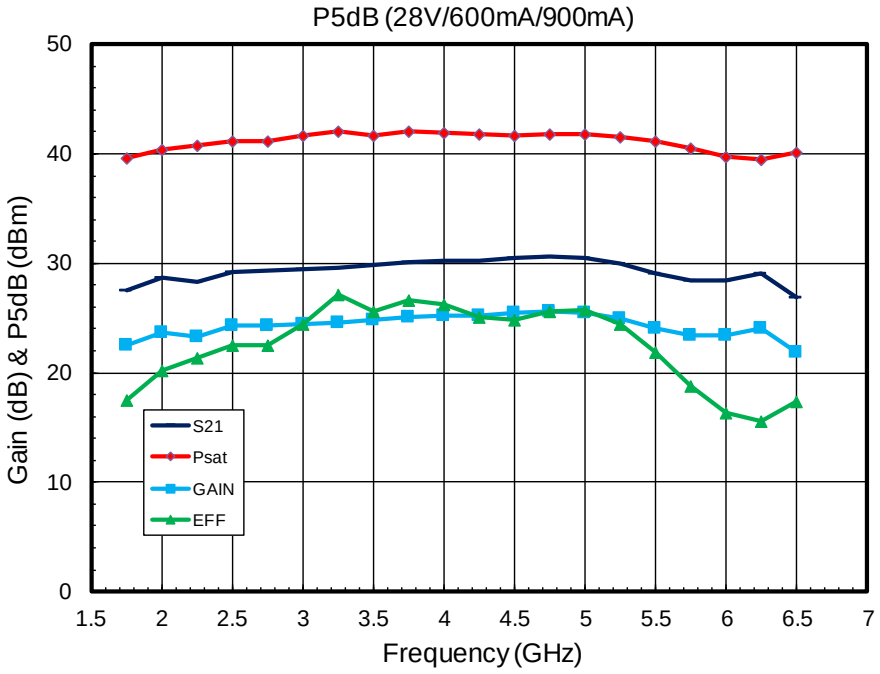
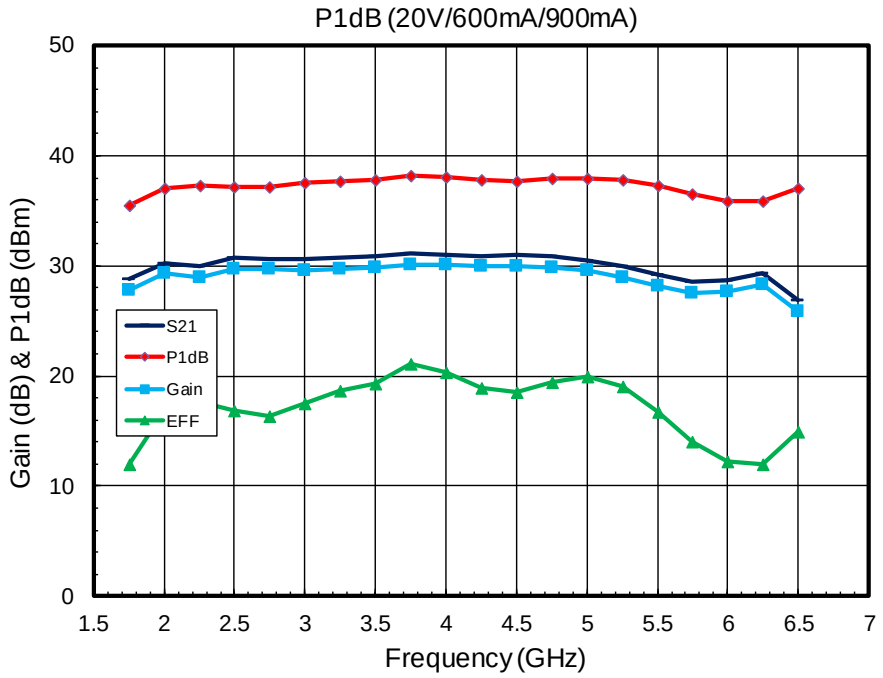
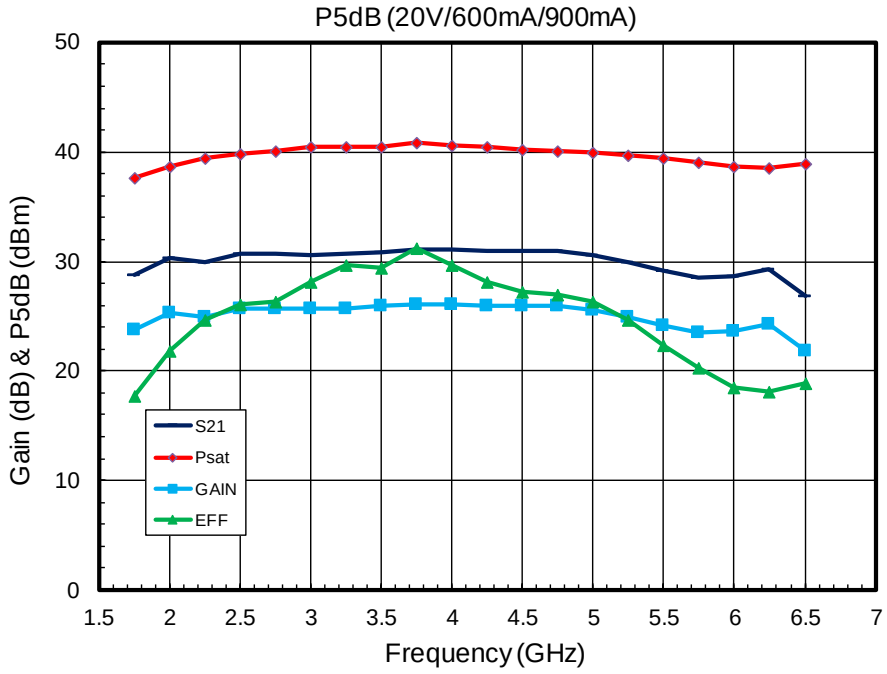
POWER DATA**





** Power measured using test fixture. Bias is $V_{ds1} = V_{ds2} = V_{ds3}$=+28V, $I_{ds1} + I_{ds2}$=600mA, I_{ds3}=900mA , $V_{gs1} = V_{gs2} = V_{gs3}$ =-2.0V . Gain in the two graphs is the compressed gain at 1dB and 5dB compression respectively.


P1dB (20V/600mA/900mA)
Gain (dB) & P1dB (dBm)
Frequency (GHz)
S21
P1dB
Gain
EFF
0
10
20
30
40
50
1.5
2
2.5
3
3.5
4
4.5
5
5.5
6
6.5
7


P5dB (20V/600mA/900mA)
Gain (dB) & P5dB (dBm)
Frequency (GHz)
S21
Psat
GAIN
EFF
0
10
20
30
40
50
1.5
2
2.5
3
3.5
4
4.5
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5.5
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6.5
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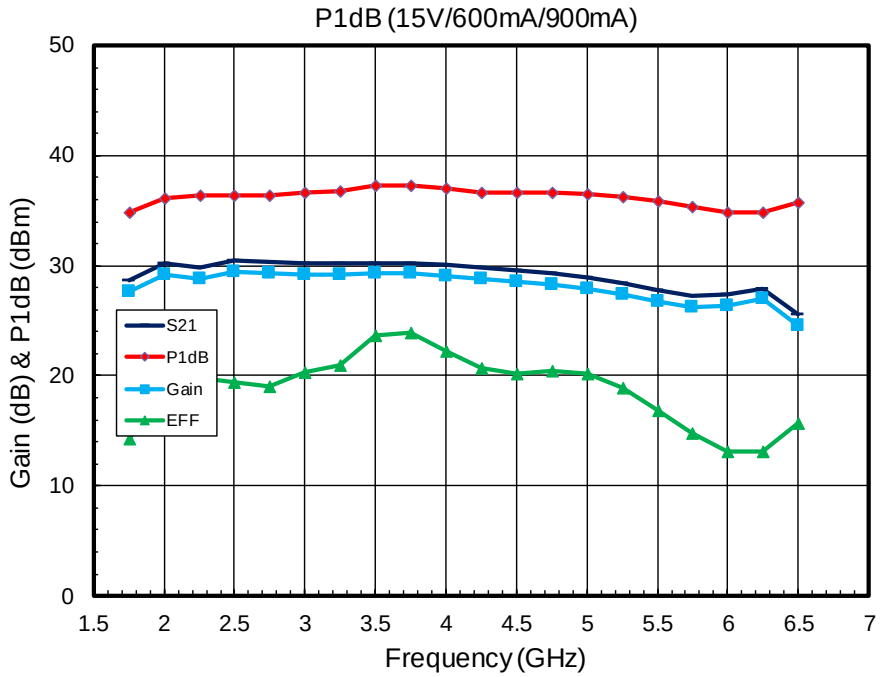
P1dB (15V/600mA/900mA)
Gain (dB) & P1dB (dBm)
Frequency (GHz)
S21
P1dB
Gain
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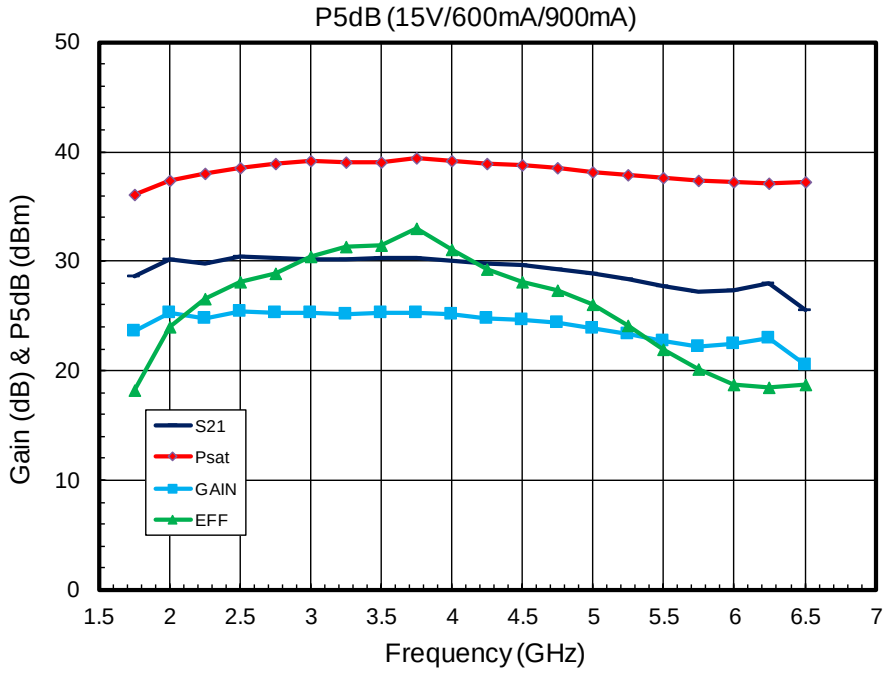
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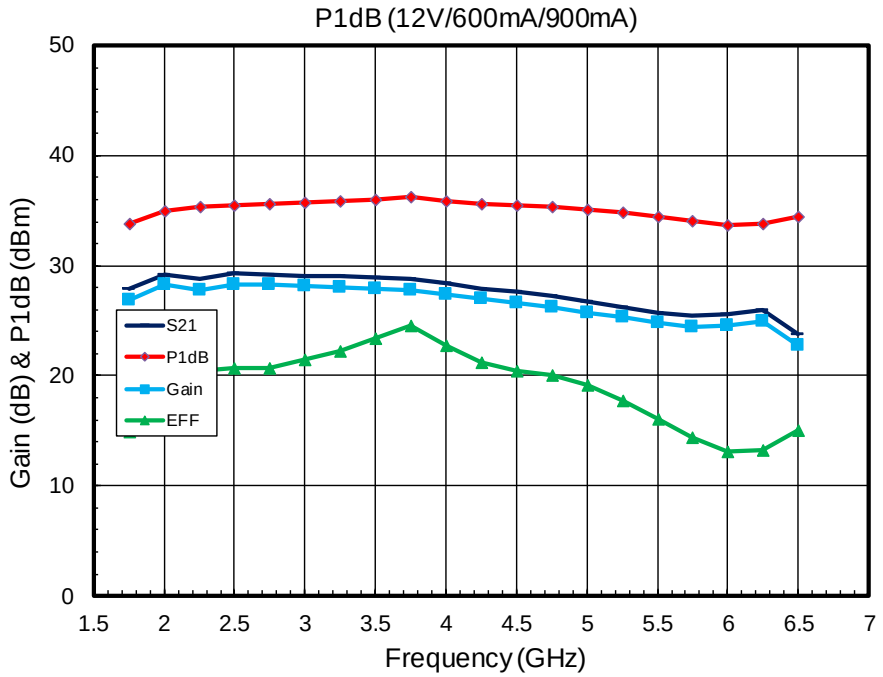
P1dB (12V/600mA/900mA)
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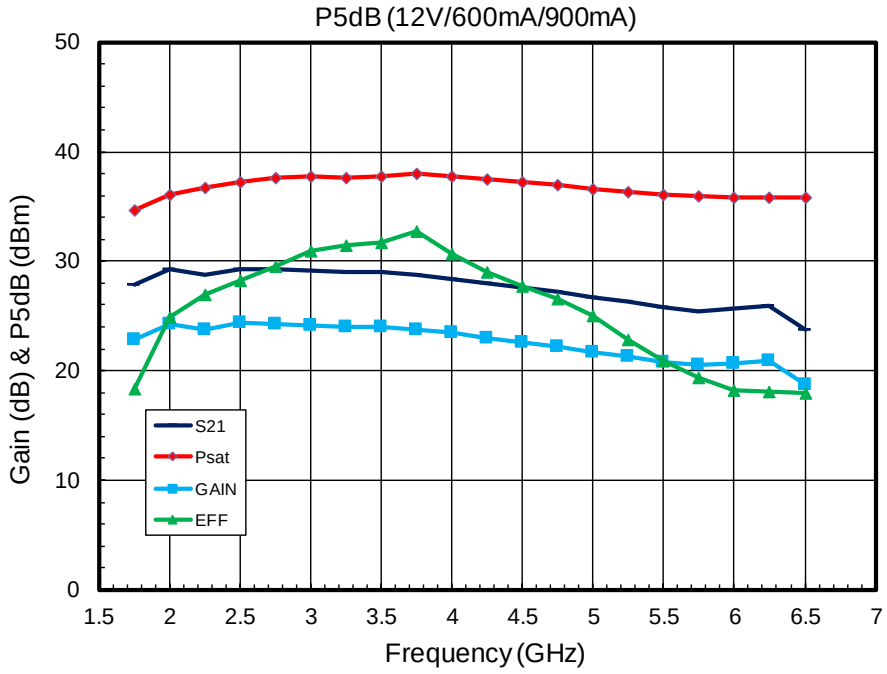
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Gain (dB) & P5dB (dBm)
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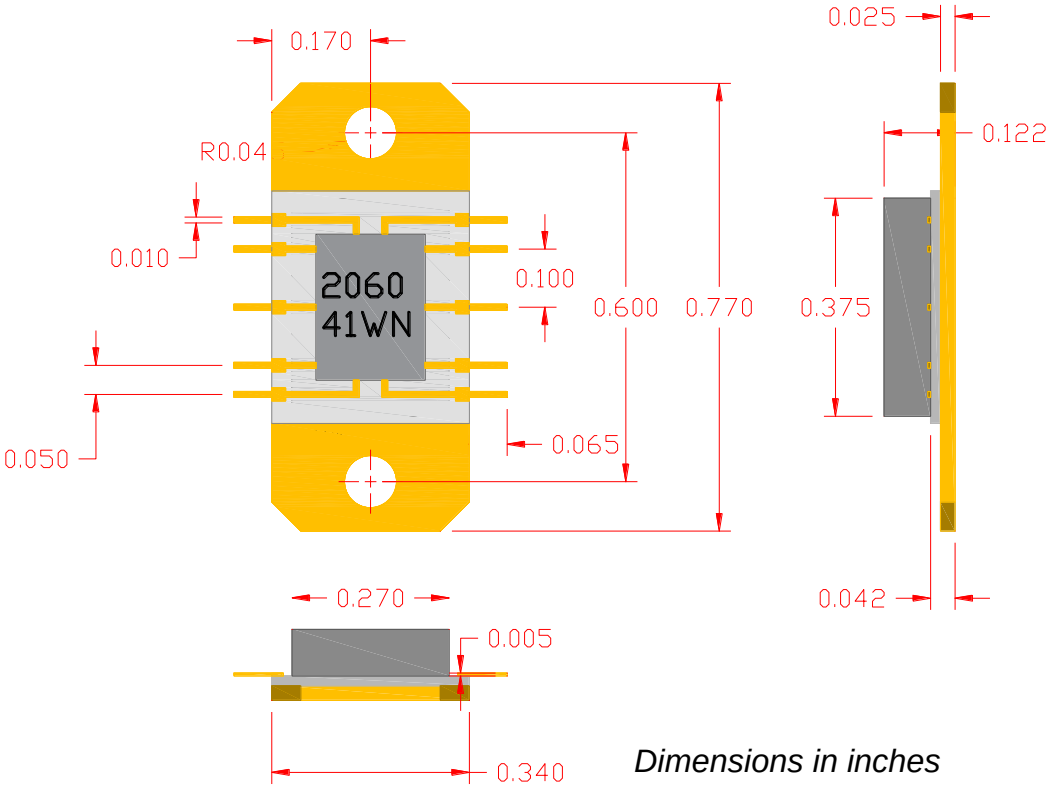
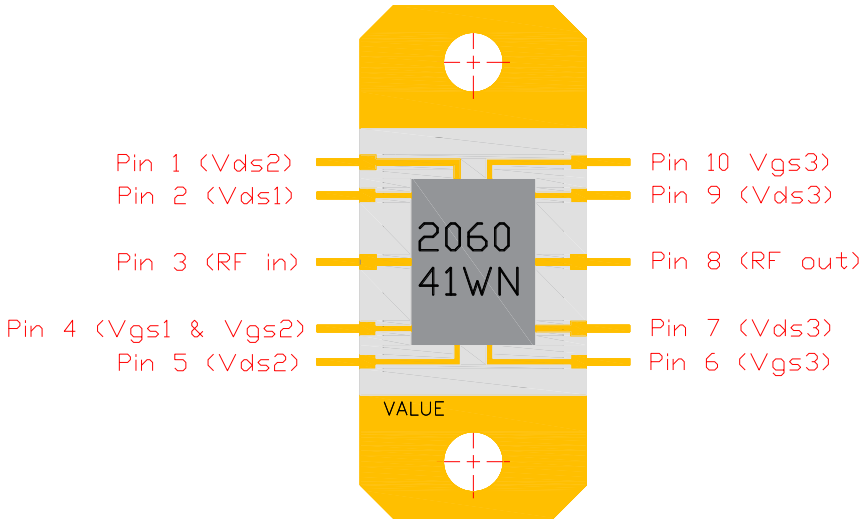
PACKAGE OUTLINE



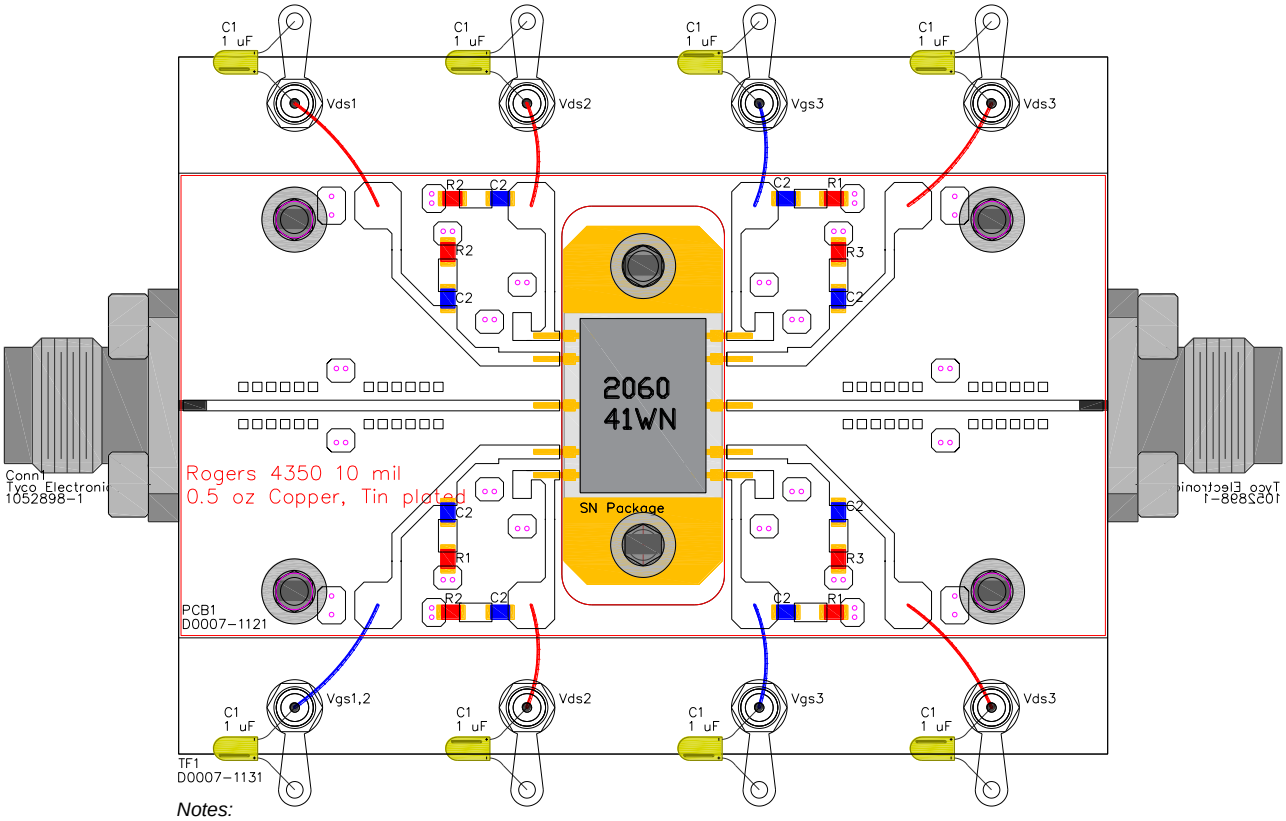
Dimensions in inches

Pin Layout



Pin No.	Function	Bias
1	Vds2	+28V
2	Vds1	+28V
3	RF in	-
4	Vgs1 & Vgs2	-2.3V
5	Vds2	+28V
6	Vgs3	-2.3V
7	Vds3	+28V
8	RF out	-
9	Vds3	+28V
10	Vgs3	-2.3V

TEST CIRCUIT



Notes:
1- Use epoxy to mount PCB
2- C1=1uF, C2=1000pF, R1=50ohms, R2=10ohms, R3=5ohms
3- All SMT Caps & Resistors are 0603 size
4- Use Test Block No. D0007-1131

Important Notes:

1- Recommended current biases are 600mA for the first & second stage and 900mA for the third stage. Gate biases of -2.0V are for reference only. V_{gs1} & V_{gs2} could be adjusted to vary the currents going thru the first stage (V_{ds1} pin) & second stage (V_{ds2} pin). V_{gs3} could be adjusted to vary the currents going the third stage thru the two V_{ds3} pins.

2- Do not apply V_{ds1}, V_{ds2} & V_{ds3} without proper negative voltages on V_{gs1} , V_{gs2} & V_{gs3}. Otherwise MMIC would fail due to excess heat.